

**UT48N12M**

Preliminary

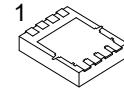
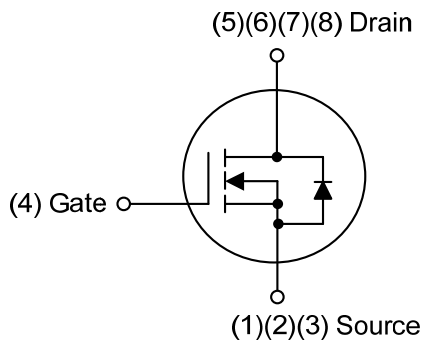
POWER MOSFET**48A, 120V N-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **UT48N12M** is a N-channel enhancement MOSFET using UTC's advanced technology to provide the customers with perfect $R_{DS(ON)}$ and high switching speed.

The UTC **UT48N12M** is suitable for all commercial-industrial applications at power dissipation levels to approximately 50 watts, etc.

FEATURES

- * $R_{DS(ON)} \leq 20 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=24\text{A}$
- * $R_{DS(ON)} \leq 26 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=24\text{A}$
- * High Switching Speed

SYMBOL

PDFN5×6

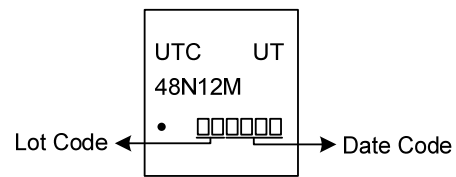
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT48N12ML-P5060-R	UT48N12MG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT48N12MG-P5060-R	(1) Packing Type	(1) R: Tape Reel
	(2) Package Type	(2) P5060: PDFN5×6
	(3) Green Package	(3) G: Halogen Free and Lead Free, K: Lead Free

■ MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	120	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	48	A
	Pulsed	I_{DM}	96	A
Avalanche Energy	Single Pulsed	E_{AS}	122.5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.6	V/ns
Power Dissipation		P_D	18	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 49.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	83	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	6.9	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR4 substrate P_C board, 2oz copper, with 1inch square copper plate.

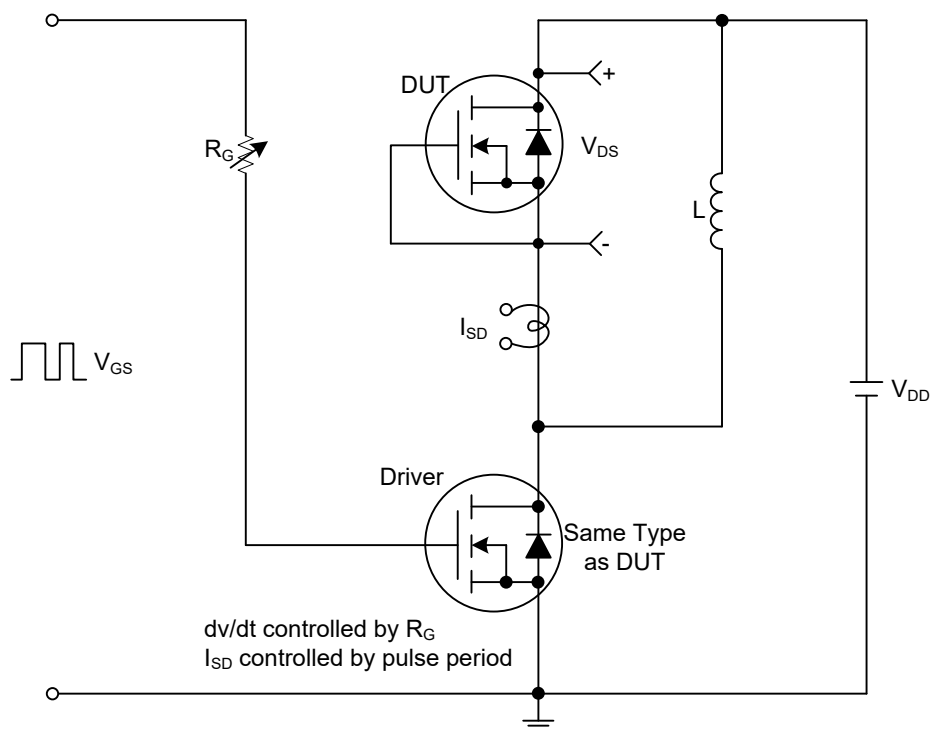
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	120			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =120V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =24A			20	mΩ
			V _{GS} =4.5V, I _D =24A			26	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1MHz		4176		pF
Output Capacitance		C _{OSS}			286		pF
Reverse Transfer Capacitance		C _{RSS}			239		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =96V, V _{GS} =10V, I _D =48A (Note 1, 2)		122		nC
Gate to Source Charge		Q _{GS}			13		nC
Gate to Drain Charge		Q _{GD}			48		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DD} =60V, V _{GS} =10V, I _D =48A, R _G =3Ω (Note 1, 2)		14		ns
Rise Time		t _R			21		ns
Turn-OFF Delay Time		t _{D(OFF)}			60		ns
Fall Time		t _F			28		ns
SOURCE DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body Diode Continuous Current		I _S				48	A
Maximum Body Diode Pulsed Current		I _{SM}				96	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =48A, V _{GS} =0V			1.4	V
Reverse Recovery Time		t _{rr}	V _{GS} =0V, I _S =30A		100		ns
Reverse Recovery Charge (Note 1)		Q _{rr}	dI _S /dI _t =100A/μs		229		nC

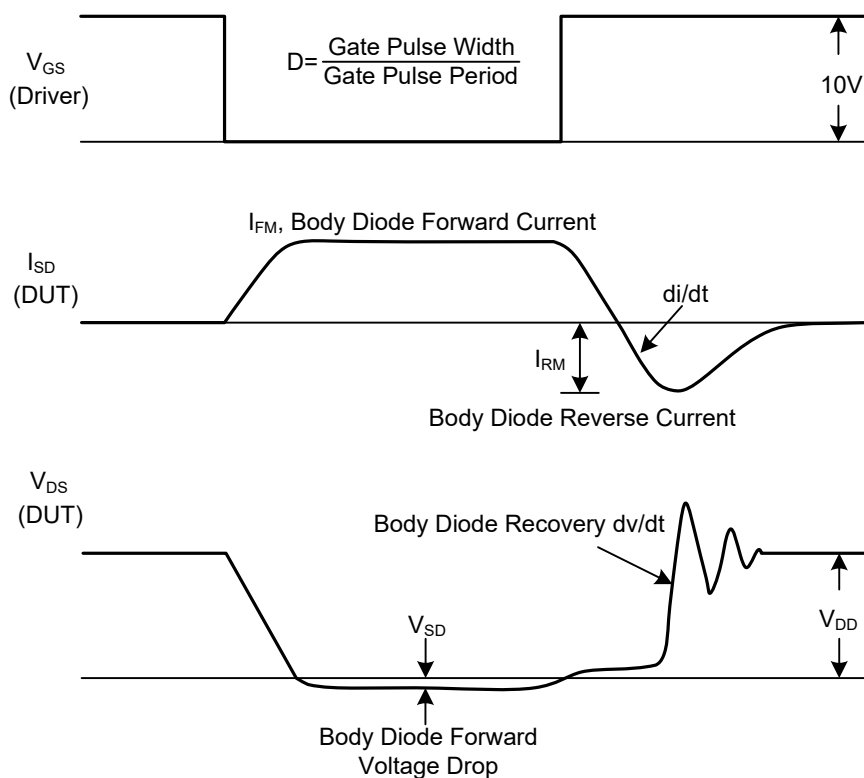
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



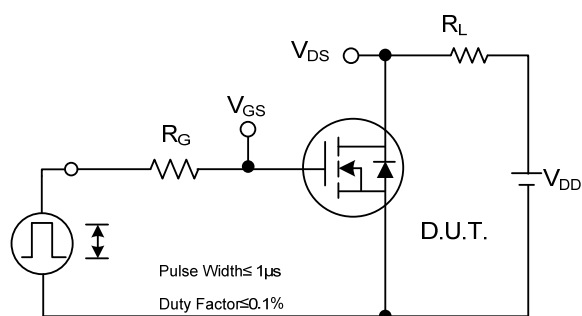
Peak Diode Recovery dv/dt Test Circuit



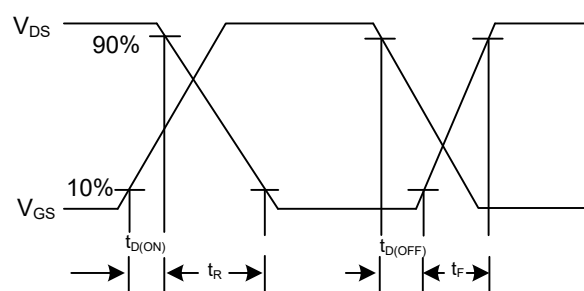
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

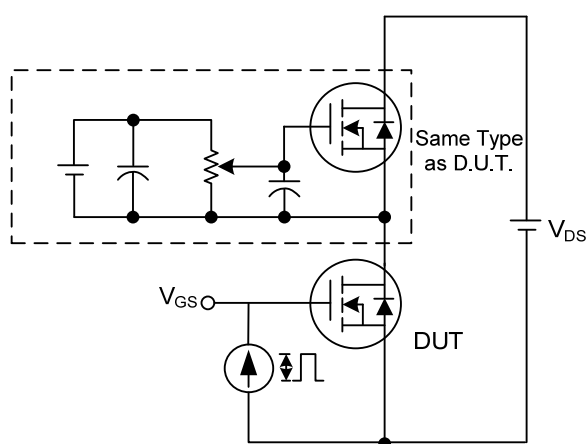
■ TEST CIRCUITS AND WAVEFORMS



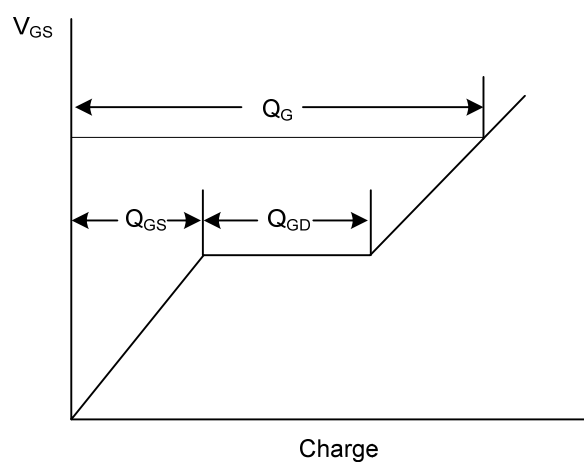
Switching Test Circuit



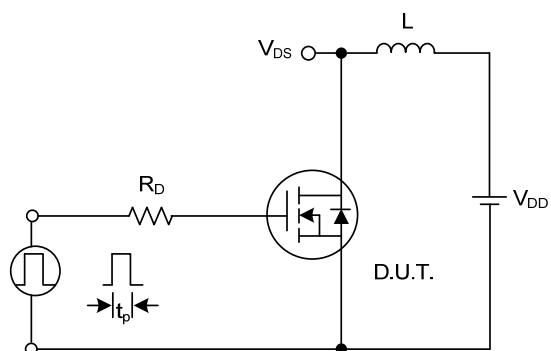
Switching Waveforms



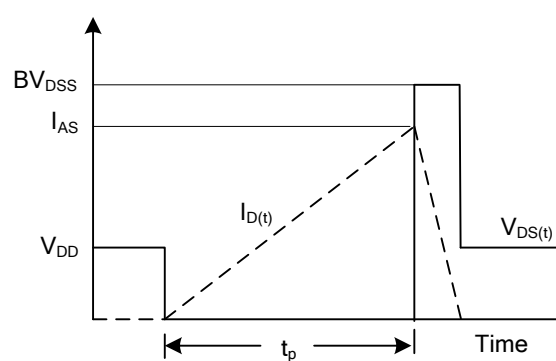
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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