



UT1N10

Power MOSFET

1.0A, 100V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

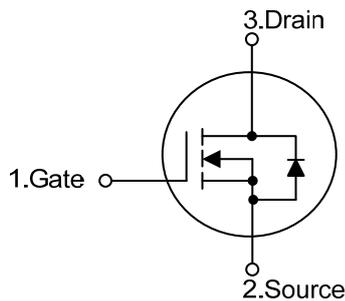
DESCRIPTION

The UTC **UT1N10** is a N-channel power MOSFET providing very low on-resistance. It has high efficiency and perfect cost-effectiveness. It can be generally applied in the commercial and industrial fields.

FEATURES

- * $R_{DS(ON)} \leq 0.5 \Omega @ V_{GS}=10V, I_D=0.5A$
- $R_{DS(ON)} \leq 0.55 \Omega @ V_{GS}=4.5V, I_D=0.5A$
- * Simple drive requirement

SYMBOL

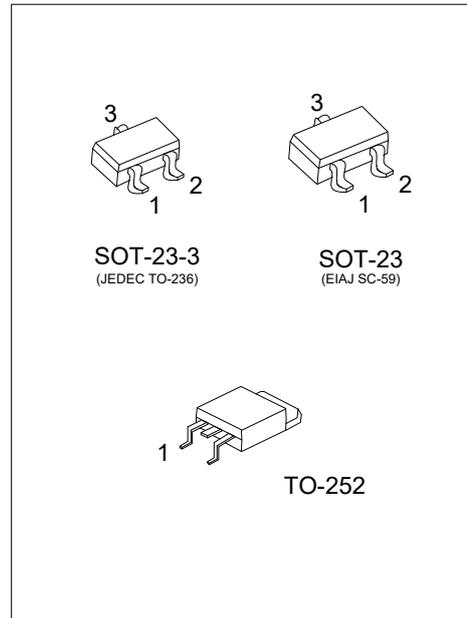


ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT1N10L-AE2-R	UT1N10G-AE2-R	SOT-23-3	G	S	D	Tape Reel
UT1N10L-AE3-R	UT1N10G-AE3-R	SOT-23	G	S	D	Tape Reel
UT1N10L-TN3-R	UT1N10G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain

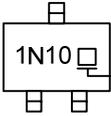
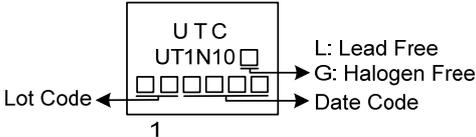
<p>UT1N10G-AE2-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) AE2: SOT-23-3, AE3: SOT-23, TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

SOT-23 / SOT-23-3	TO-252
 <p>A schematic diagram of a SOT-23 or SOT-23-3 package. It is a small rectangle with three leads: one on the top, one on the right, and two on the bottom. The text "1N10" is printed on the top surface. To the right of the package, an arrow points to the text "L: Lead Free" and "G: Halogen Free".</p>	 <p>A schematic diagram of a TO-252 package. It is a larger rectangle with a central square area. The text "UTC" and "UT1N10" are printed on the top surface. Below the package, there are five small squares representing a lot code, with an arrow pointing left to the text "Lot Code". To the right of the package, an arrow points to the text "L: Lead Free", "G: Halogen Free", and "Date Code". A small number "1" is printed below the package.</p>

■ ABSOLUTE MAXIMUM RATING (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	100	V
Gate-Source Voltage		V _{GSS}	±20	V
Drain Current	Continuous	I _D	1	A
	Pulsed (Note 2)	I _{DM}	2	A
Peak Diode Recovery dv/dt (Note 3)		dv/dt	1.9	V/ns
Power Dissipation (T _A =25°C)	SOT-23-3/SOT-23	P _D	0.3	W
	TO-252		1.5	W
Junction Temperature		T _J	+150	°C
Storage Temperature Range		T _{STG}	-55 ~ +150	°C

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
 3. I_{SD} ≤ 1.0A, di/dt ≤ 100 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J = 25°C.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-23-3/SOT-23	θ _{JA}	416 (Note)	°C/W
	TO-252		83.3 (Note)	°C/W

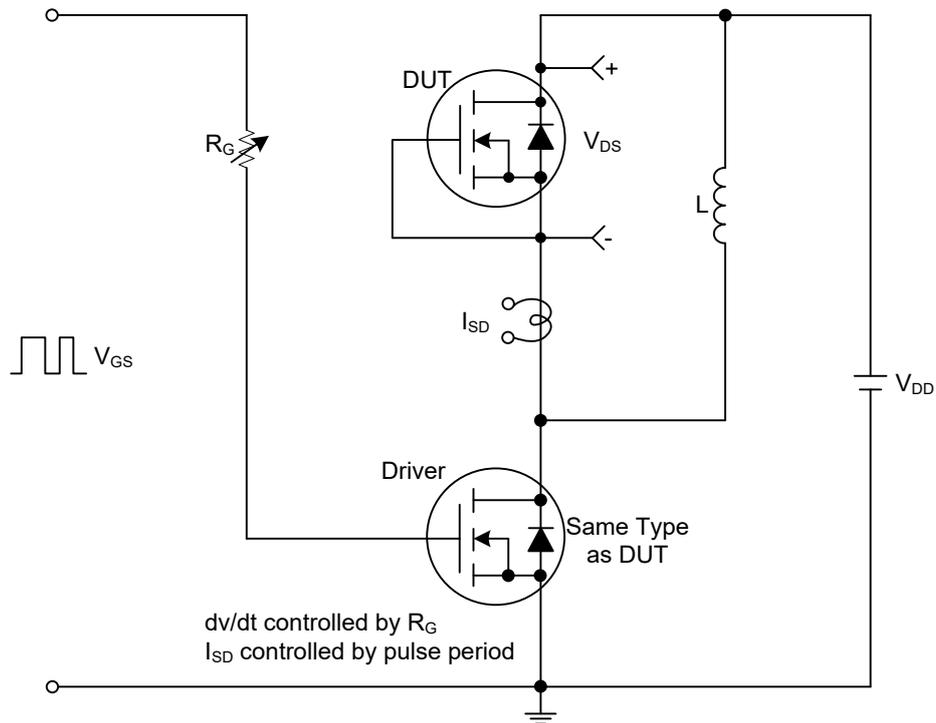
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

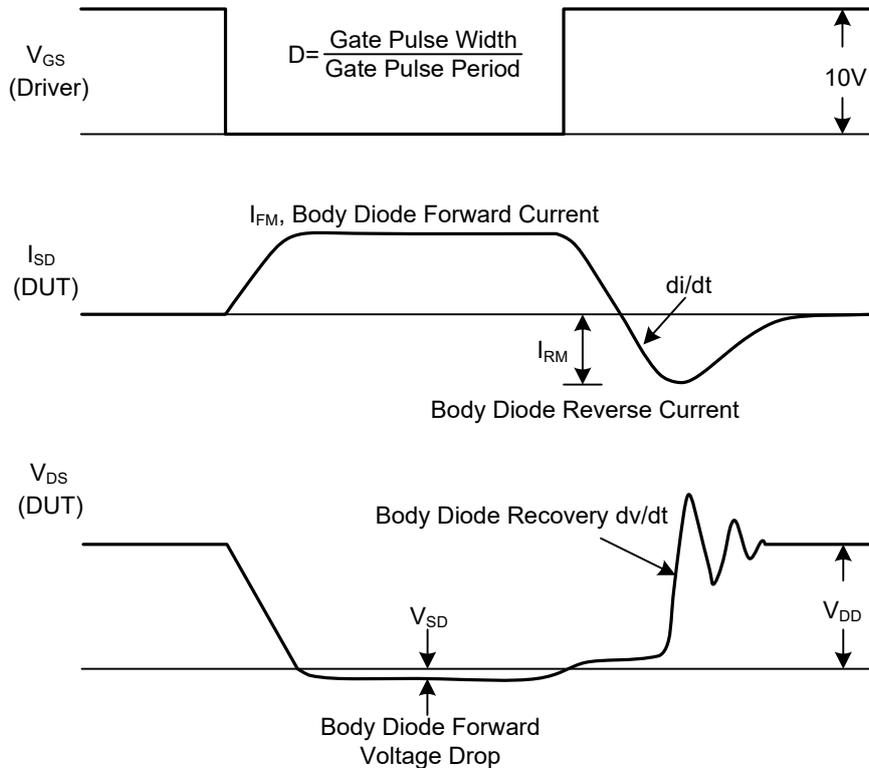
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	100			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Drain to Source On-state Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =0.5A			0.5	Ω
		V _{GS} =4.5V, I _D =0.5A			0.55	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		150		pF
Output Capacitance	C _{OSS}			18		pF
Reverse Transfer Capacitance	C _{RSS}				12	
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q _G	V _{DS} =80V, V _{GS} =10V, I _D =1A, I _G =1mA (Note 1, 2)		10		nC
Gate Source Charge	Q _{GS}			2		nC
Gate Drain Charge	Q _{GD}			1.6		nC
Turn-ON Delay Time (Note 1)	t _{D(ON)}	V _{DD} =50V, V _{GS} =10V, I _D =1A, R _G =25Ω (Note 1, 2)		4		ns
Turn-ON Rise Time	t _R			18		ns
Turn-OFF Delay Time	t _{D(OFF)}			14		ns
Turn-OFF Fall-Time	t _F			19		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =1A, V _{GS} =0V			1.4	V
Reverse Recovery Time (Note 1)	t _{rr}	I _S =1A, V _{GS} =0V, di/dt=100A/μs		32		ns
Reverse Recovery Charge	Q _{rr}			14		nC

- Notes: 1. Pulse Test : Pulse width ≤ 1000μs, Duty cycle ≤ 2%.
 2. Essentially independent of operating ambient temperature.

TEST CIRCUITS AND WAVEFORMS



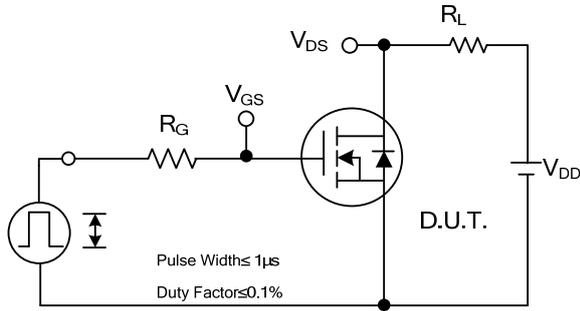
Peak Diode Recovery dv/dt Test Circuit



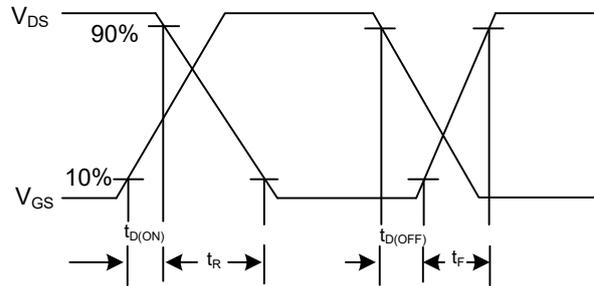
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

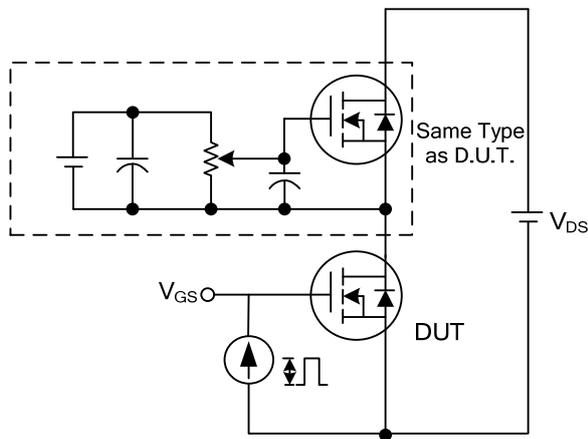
TEST CIRCUITS AND WAVEFORMS



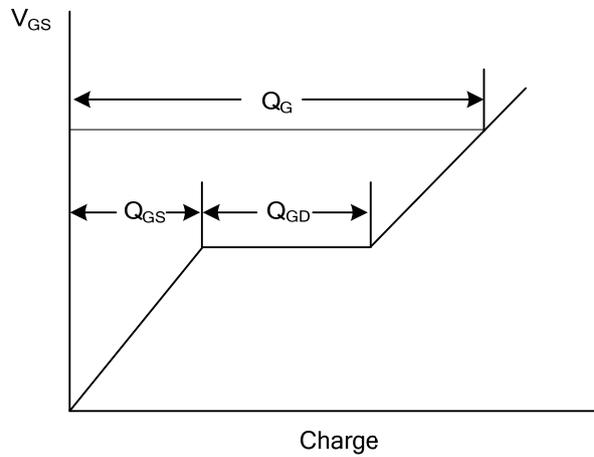
Switching Test Circuit



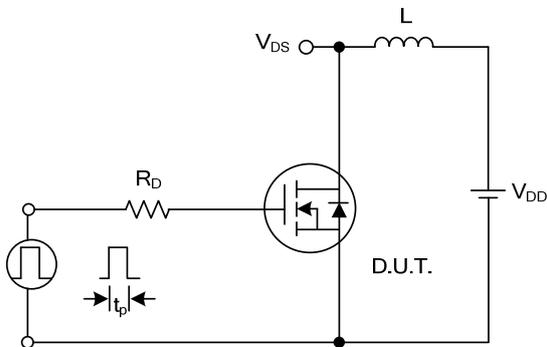
Switching Waveforms



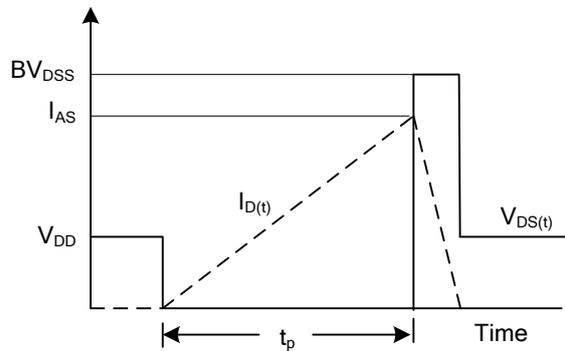
Gate Charge Test Circuit



Gate Charge Waveform

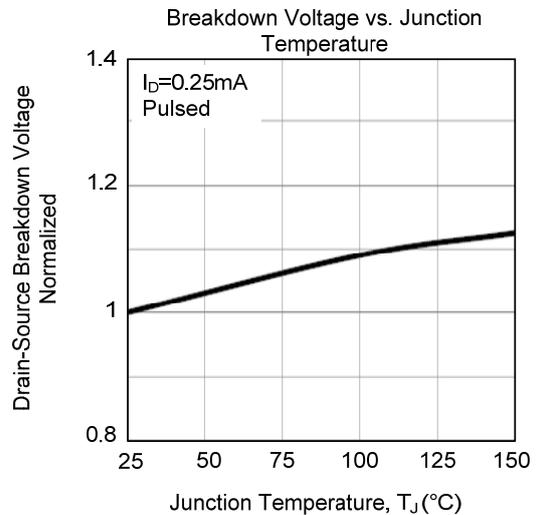
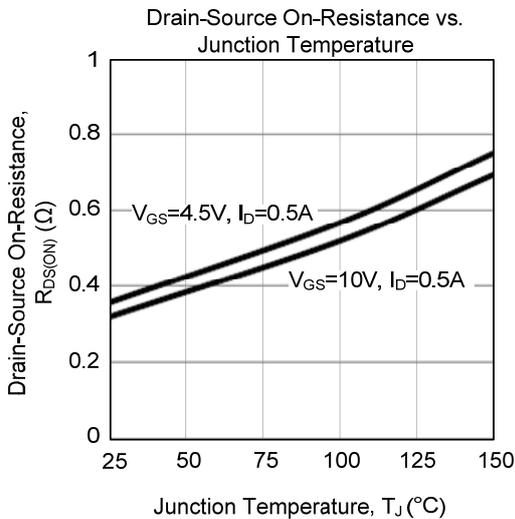
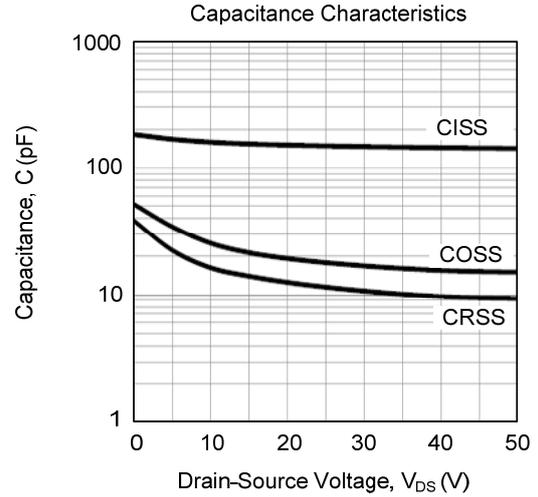
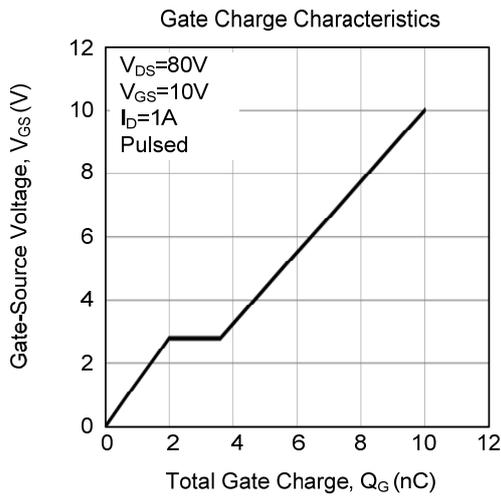
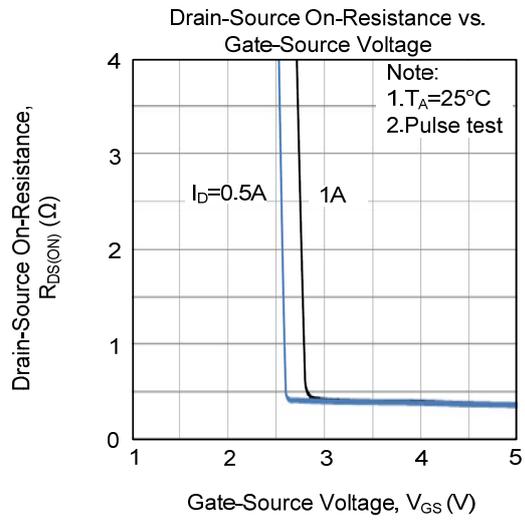
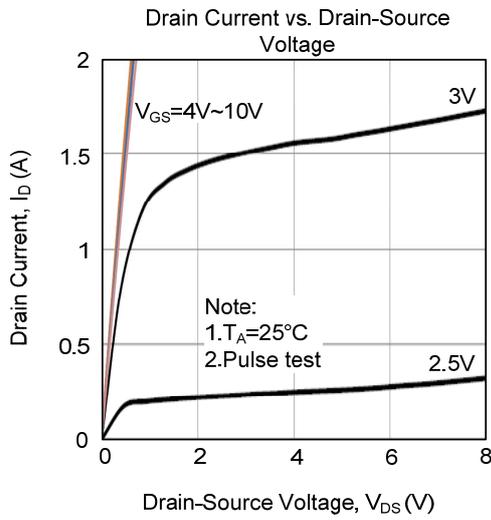


Unclamped Inductive Switching Test Circuit

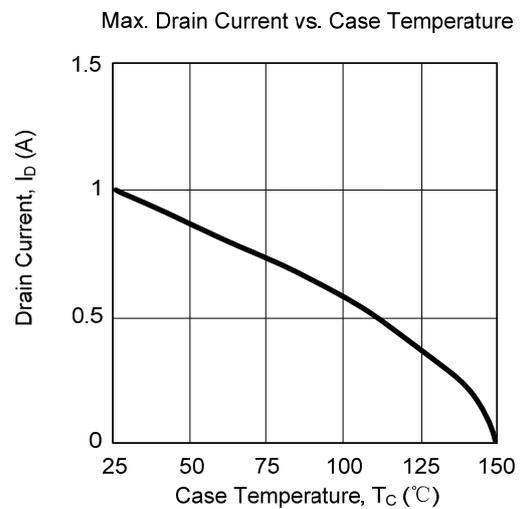
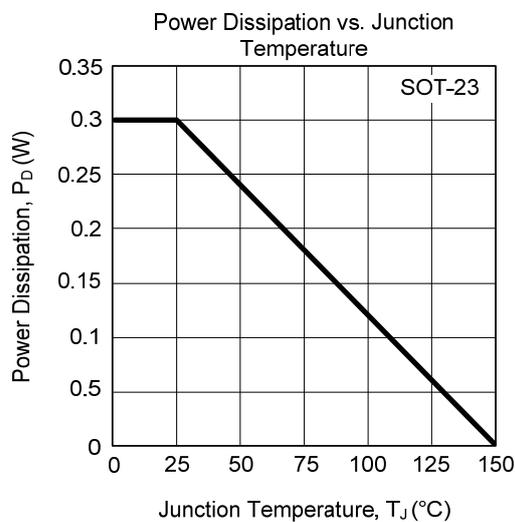
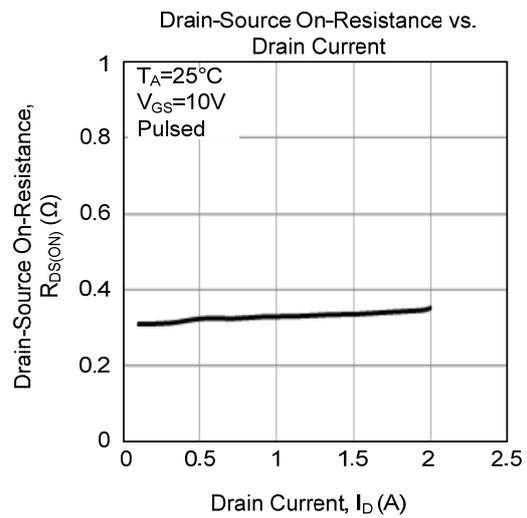
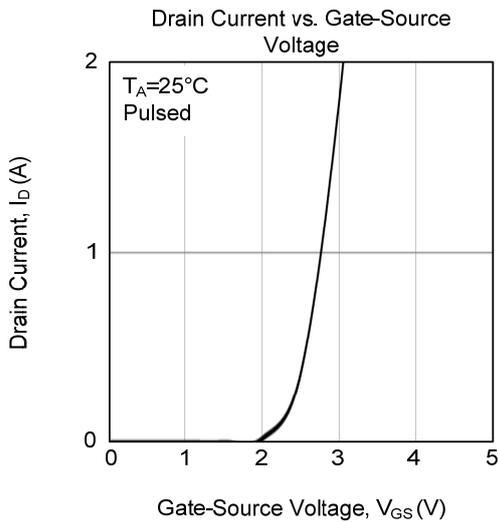
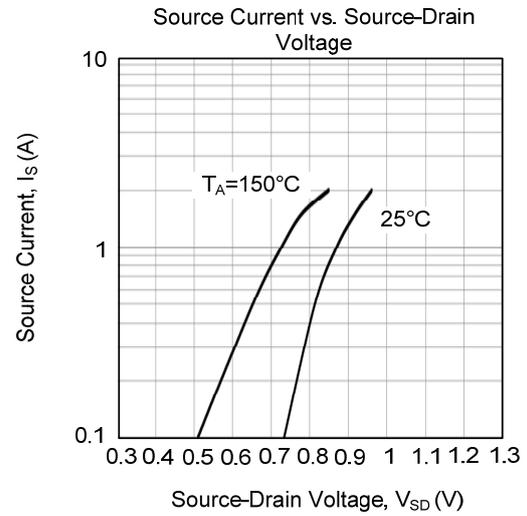
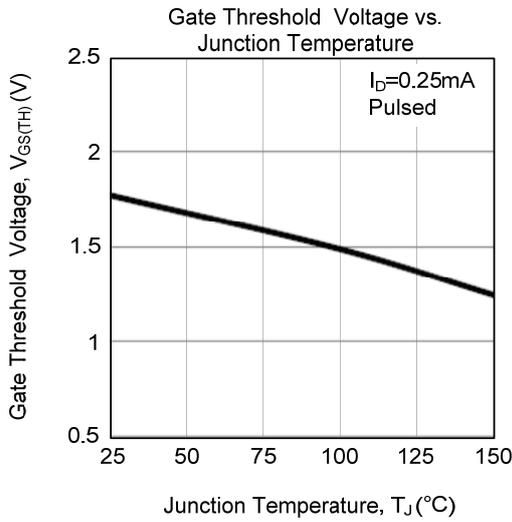


Unclamped Inductive Switching Waveforms

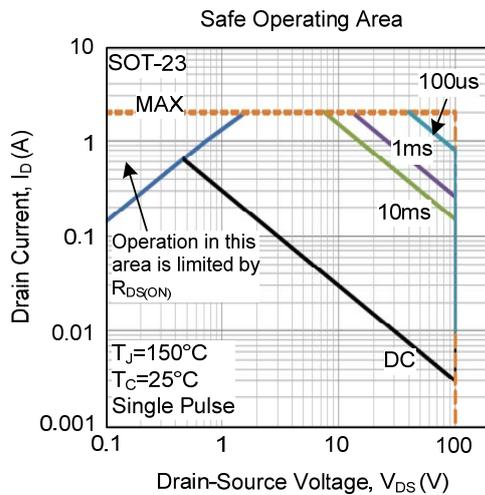
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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