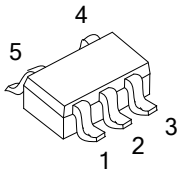
USRC8801 **Advance** ***CMOS IC***

FAST TURN-OFF INTELLIGENT CONTROLLER



SOT-25

■ DESCRIPTIO

The **USRC8801** is a Low-Drop Diode Emulator IC that, combined with an external switch replaces Schottky diodes in high-efficiency, Flyback converters. The chip regulates the forward drop of an external switch to about 70mV and switches it off as soon as the voltage becomes negative.

■ FEATURES

* Works with both Standard and Logic Level FETS
* Compatible with Energy Star, 1W Standby Requirements
* V_{DD} Range From 8V to 24V
* 70mV VDS Regulation Function
* Fast Turn-off Total Delay of 20ns
* Max 400kHz Switching Frequency
* <3mA Low Quiescent Current
* Supports CCM, DCM and Quasi-Resonant Topologies
* Supports High-side and Low-side Rectification
* Power Savings of Up to 1.5W in a Typical Notebook Adapter

■ APPLICATION

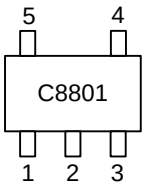
* Industrial Power Systems
* Distributed Power Systems
* Battery Powered Systems
* Flyback Converters

■ ORDERING INFORMATION

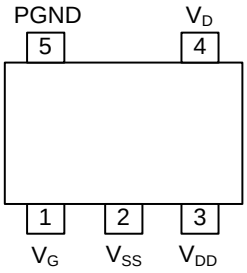
Ordering Number		Package	Packing
Lead Free	Halogen Free		
USRC8801L-AF5-R	USRC8801G-AF5-R	SOT-25	Tape Reel

USRC8801G-AF5-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AF5: SOT-25 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



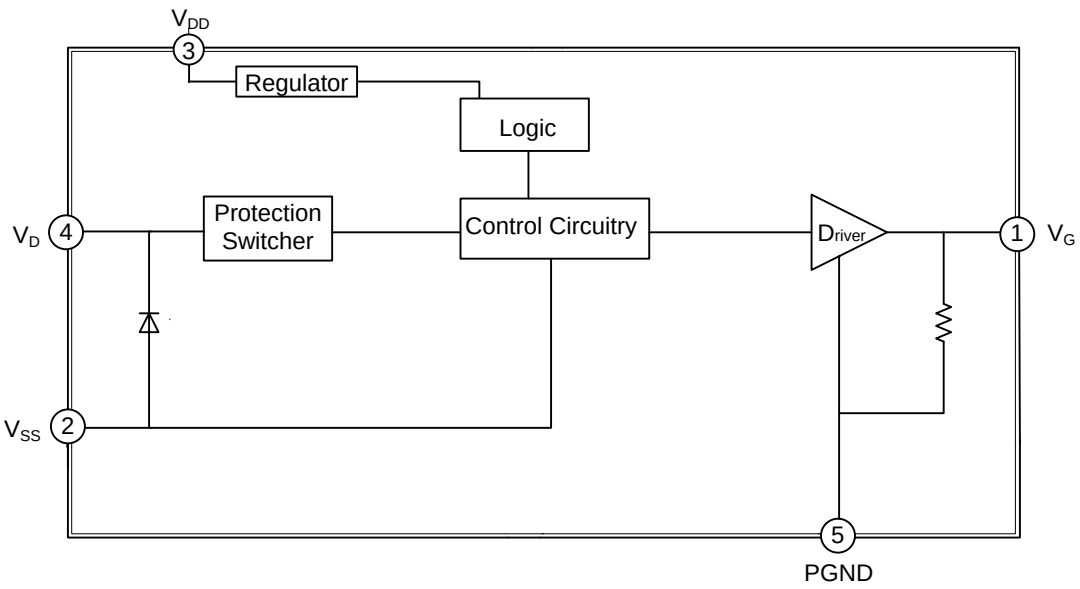
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	TYPE	DESCRIPTION
1	V_G		Gate drive output
2	V_{SS}	I	Ground，also used as reference for VD
3	V_{DD}	I	Supply Voltage
4	V_D	I/O	FET drain voltage sense
5	PGND	I/O	Power Ground,return for driver switch

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{DD} to V_{SS}	V_{DD}-V_{SS}	-0.3 ~ +27	V
PGND to V_{SS}	V_{PGND}-V_{SS}	-0.3 ~ +0.3	V
V_G to V_{SS}	V_G-V_{SS}	-0.3 ~ V_{CC}	V
V_D to V_{SS}	V_D-V_{SS}	-0.7 ~ +180	V
EN to V_{SS}	V_{EN}-V_{SS}	-0.3 ~ +6.5	V
Maximum Operating Frequency	f_{MAX}	400	kHz
Power Dissipation	P_D	0.57	W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-55 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
V_{DD} to V_{SS}	V_{IN}	8 ~ 24	V
Operating Junction Temperature	T_J	-40 ~ +125	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	220	°C/W
Junction to Case	θ_{JC}	110	°C/W

■ ELECTRICAL CHARACTERISTICS (V_{DD}=12V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} Voltage Range	V_{DD}		8		24	V
V_{DD} UVLO Rising	V_{UVLO}		5.0	6.0	7.0	V
V_{DD} UVLO Hysteresis	V_{UVLO_HS}			1.2		V
Operating Current	I_{CC}	C_{LOAD}=5nF, F_{SW}=100kHz		8	12	mA
Quiescent Current	I_{NS}	No Switching		2	3	mA
Shutdown Current	I_{SD}	V_{DD} =4 V		100	150	μA
V_{DD}=20V	I_{EN}	EN=0V (50 kΩ)			250	μA
Thermal Shutdown	T_{SD}			170		°C
Thermal Shutdown hysteresis	T_{HS}			50		°C
CONTROL CIRCUITRY SECTION						
V_{SS}–V_D Forward Voltage, Vfwd	V_{FWD}		55	70	85	mV
Turn-on Delay	T_D	C_{LOAD}=5nF		150		ns
		C_{LOAD}=10nF		200		ns
Pull-down Resistance of V_G Pin	R_{PD}			10	20	kΩ
Input Bias Current On V_D Pin	I_{IN}	-0.3V>V_D>180V			10	uA
Minimum On-time	T_{ON}	C_{LOAD}=5nF		1.6		us
GATE DRIVER SECTION						
V_G (Low)	V_{GL}	I_{LOAD}=1mA		0.05	0.5	V
V_G (High)	V_{GH}	V_{DD}>17V	12	13.5	15	V
		V_{DD}<17V	V_{DD}-2.2			V
Turn-off Threshold (V_{SS}-V_D)	V_{SS}-V_D		20	30	40	mV
Turn-off Propagation delay	T_{GP}	V_D=V_{SS},R_{GATE}=0Ω		15		ns
Turn-off Total Delay	T_{GD}	V_D=V_{SS},C_{LOAD}=5nF, R_{GATE}=0Ω		20	35	ns
		V_D=V_{SS},C_{LOAD}=10nF, R_{GATE}=0Ω		30	45	ns
Pull Down Impedance	R_{PD}I			1	2	Ω
Pull Down Current	I_{PD}	3V<V_G<10V		2		A

■ APPLICATION INFORMATION

The **USRC8801** supports operation in CCM, DCM and Quasi-Resonant topologies. Operating in either a DCM or Quasi-Resonant topology, the control circuitry controls the gate in forward mode and will turn the gate off when the MOSFET current is fairly low. In CCM operation, the control circuitry turns off the gate when very fast transients occur.

Blanking

The control circuitry contains a blanking function. When it pulls the MOSFET on/off, it makes sure that the on/off state at least lasts for some time. The turn on blanking time is ~1.6us, which determines the minimum on-time. During the turn on blanking period, the turn off threshold is not totally blanked, but changes the threshold voltage to ~+50mV (instead of -30mV). This assures that the part can always be turned off even during the turn on blanking period. (Albeit slower, so it is not recommended to set the synchronous period less than 1.6us at CCM condition in flyback converter, otherwise shoot through may occur)

V_D CLAMP

Because V_D can go as high as 180V, a High-Voltage JFET is used at the input. To avoid excessive currents when Vg goes below -0.7V, a small resistor is recommended between V_D and the drain of the external MOSFET.

Under-Voltage Lockout (UVLO)

When the V_{DD} is below UVLO threshold, the part is in sleep mode and the Vg pin is pulled low by a 10k Ω resistor.

Thermal shutdown

If the junction temperature of the chip exceeds 170°C, the Vg will be pulled low and the part stops switching. The part will return to normal function after the junction temperature has dropped to 120°C.

Turn-on Phase

When the synchronous MOSFET is conducting, current will flow through its body diode which generates a negative V_{DS} across it. Because this body diode voltage drop (<-500mV) is much smaller than the turn on threshold of the control circuitry (-70mV), which will then pull the gate driver voltage high to turn on the synchronous MOSFET after about 150ns turn on delay.

As soon as the turn on threshold (-70mV) is triggered, a blanking time (Minimum on-time: ~1.6us) will be added during which the turn off threshold will be changed from -30mV to +50mV. This blanking time can help to avoid error trigger on turn off threshold caused by the turn on ringing of the synchronous MOSFET.

Conducting Phase

When the synchronous MOSFET is turned on, Vds becomes to rise according to its on resistance, as soon as V_{DS} rises above the turn on threshold (-70mV), the control circuitry stops pulling up the gate driver which leads the gate voltage is pulled down by the internal pull-down resistance (10kΩ) to larger the on resistance of synchronous MOSFET to ease the rise of V_{DS}.

By doing that, V_{DS} is adjusted to be around -70mV even when thecurrent through the MOS is fairly small, this function can make the driver voltage fairly low when the synchronous MOSFET is turned off to fast the turn off speed (this function is still active during turn on blanking time which means the gate driver could still be turned off even with very small duty of the synchronous MOSFET).

Turn-off Phase

When V_{DS} rises to trigger the turn off threshold (-30mV), the gate voltage is pulled to low after about 20ns turn off delay by the control circuitry. Similar with turn-on phase, a 200ns blanking time is added after the synchronous MOSFET is turned off to avoid error trigger.

Due to the high current, the gate driver will be saturated at first. After V_{DS} goes to above -70mV, gate driver voltage decreases to adjust the V_{DS} to typical -70mV.

Due to the low current, the gate driver voltage never saturates but begins to decrease as soon as the synchronous MOSFET is turned on and adjust the V_{DS}.

■ APPLICATION INFORMATION (Cont.)

SR MOSFET Selection and Driver ability

The Power MOSFET selection proved to be a trade off between Ron and Qg. In order to achieve high efficiency, the MOSFET with smaller Ron is always preferred, while the Qg is usually larger with smaller Ron, which makes the turn-on/off speed lower and lead to larger power loss. For **USRC8801**, because V_{DS} is regulated at ~ -70mV during the driving period, the MOSFET with too small Ron is not recommend, because the gate driver may be pulled down to a fairly low level with too small Ron when the MOSFET current is still fairly high, which make the advantage of the low Ron inconspicuous.

Assume 50% duty cycle and the output current is I_{OUT}.

To achieve fairly high usage of the MOSFET'S Ron, it is expected that the MOSFET be fully turned on at least 50% of the SR conduction period:

$$V_{DS}= -I_C \times Ron=-2. I_{OUT} \times Ron \leq - Vfwd$$

■ TYPICAL APPLICATION CIRCUIT