



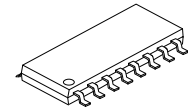
CMOS 8-STAGE SHIFT-AND-STORE BUS REGISTER

DESCRIPTION

The **UCD4094** consists of an 8-stage shift register and 8-stage D-type latch with 3-stage parallel outputs. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage QS1 can be used to cascade several devices.

The output of QS1 is transferred to a second output (QS2) on the following negative transition of the clock input signal. The data of each stage of the shift register is provided with a latch which latches data on the negative going transition of the Strobe input signal. When the strobe input is held high, data propagates through the latch to a 3-state output buffer.

The buffer is enabled when Output Enable input is taken high.



SOP-16

FEATURES

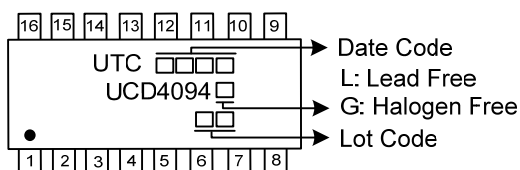
- * Operate from 3V to 18V
- * Three-state outputs
- * Standardized, symmetrical output characteristics
- * 5V, 10V and 15V parametric ratings

ORDERING INFORMATION

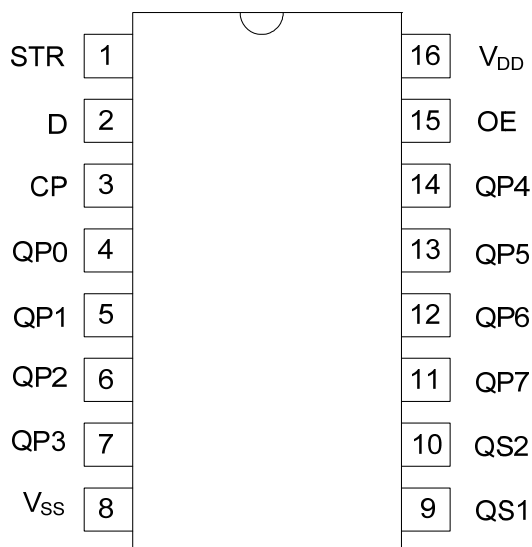
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4094L-S16-R	UCD4094G-S16-R	SOP-16	Tape Reel

UCD4094G-S16-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) S16: SOP-16
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q'6	NC
↓	L	X	X	Z	Z	NC	Q'7
↑	H	L	X	NC	NC	Q'6	NC
↑	H	H	L	L	QPn-1	Q'6	NC
↑	H	H	H	H	QPn-1	Q'6	NC
↓	H	H	H	NC	NC	NC	Q'7

Note: H : HIGH voltage level; L : LOW voltage level.

X : Don't care.

Z : High impedance OFF-state.

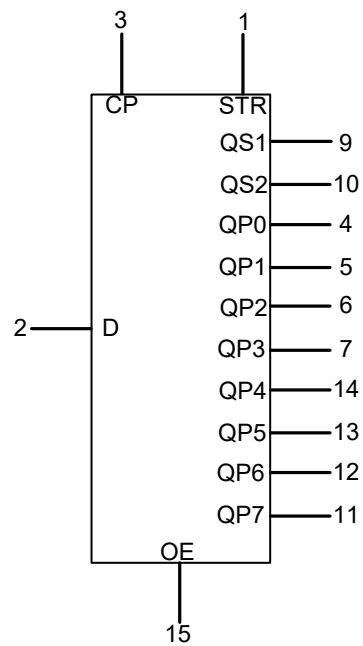
NC: No change.

↑ : Low-to-High CP transition. ↓ : High-to-Low CP transition.

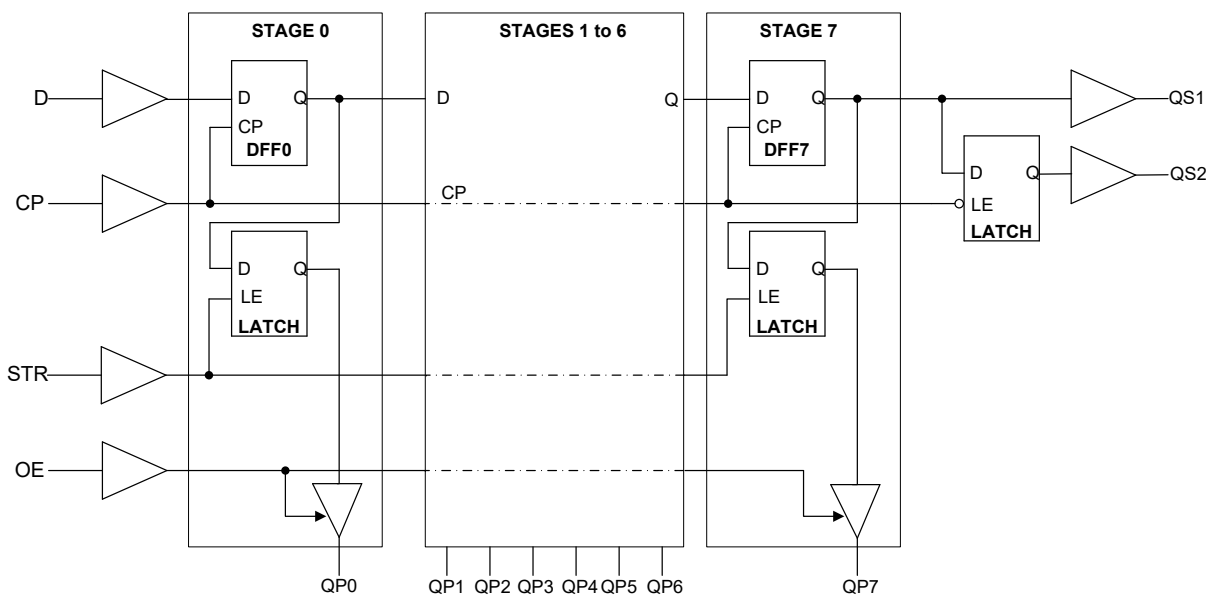
Q'6: The data in register stage 6 before the Low to High clock transition.

Q'7: The data in register stage 7 before the High to Low clock transition.

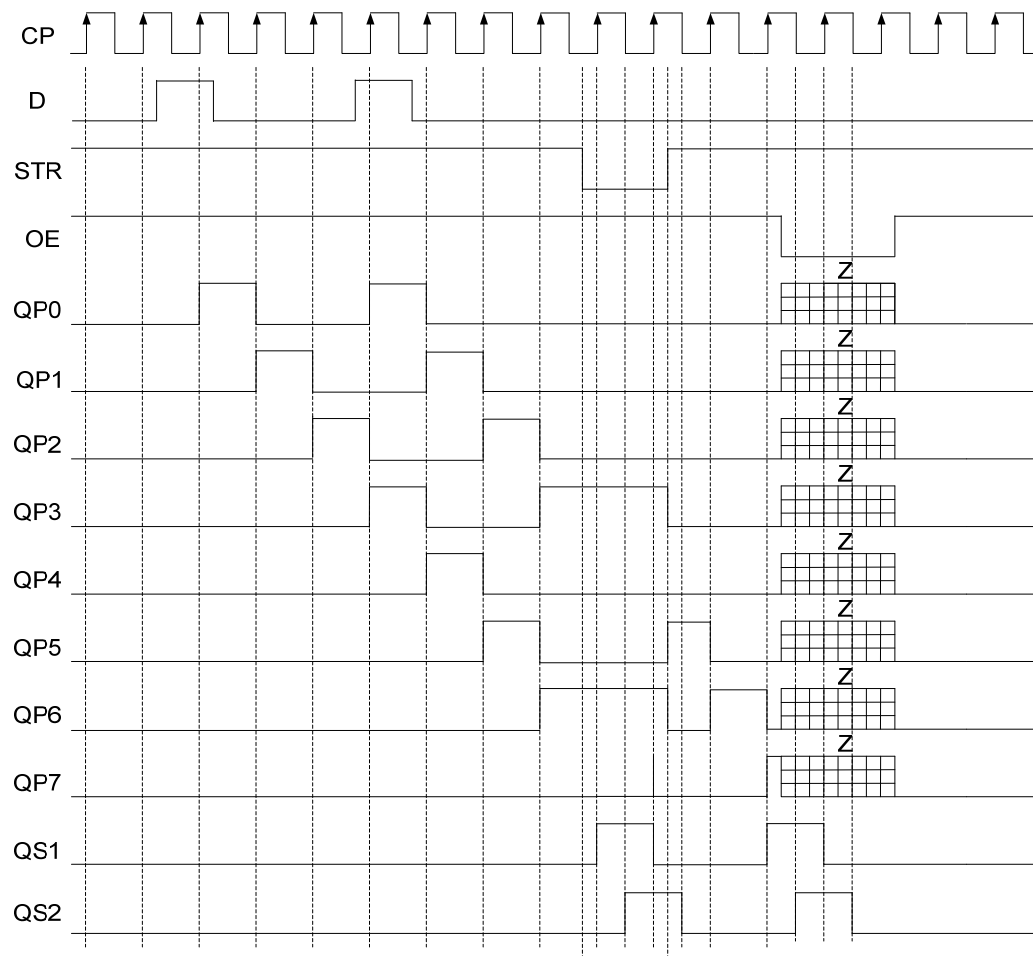
■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{DD}		-0.5 ~ +20	V
Input Voltage	V_{IN}		-0.5 ~ $V_{DD}+0.5$	V
Continuous V_{CC} or GND Current	I_{CC}		± 100	mA
Continuous Input Current	I_{IN}		± 10	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	Operating	3		18	V
Input Voltage	V_{IN}		0		V_{DD}	V
Operating Temperature	T_A		-40		+125	°C
Clock Input Rise or Fall time	t_R, t_F	$V_{DD}=5V$			15	us
		$V_{DD}=10V$			5	us
		$V_{DD}=15V$			5	us

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	$V_{DD}=5V, V_{IN}=0V$ or V_{DD}	4.95			V
		$V_{DD}=10V, V_{IN}=0V$ or V_{DD}	9.95			V
		$V_{DD}=15V, V_{IN}=0V$ or V_{DD}	14.95			V
Low-Level Output Voltage	V_{OL}	$V_{DD}=5V, V_{IN}=0V$ or V_{DD}			0.05	V
		$V_{DD}=10V, V_{IN}=0V$ or V_{DD}			0.05	V
		$V_{DD}=15V, V_{IN}=0V$ or V_{DD}			0.05	V
Input Low Voltage	V_{IL}	$V_{DD}=5V, V_{OUT}=0.5V$ or $4.5V$			1.5	V
		$V_{DD}=10V, V_{OUT}=1V$ or $9V$			3	V
		$V_{DD}=15V, V_{OUT}=1.5V$ or $13.5V$			4	V
Input High Voltage	V_{IH}	$V_{DD}=5V, V_{OUT}=0.5V$ or $4.5V$	3.5			V
		$V_{DD}=10V, V_{OUT}=1V$ or $9V$	7			V
		$V_{DD}=15V, V_{OUT}=1.5V$ or $13.5V$	11			V
High-Level Output Current	I_{OH}	$V_{DD}=5V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=2.5V$			-1.6	mA
		$V_{DD}=5V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=4.6V$			-0.51	mA
		$V_{DD}=10V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=9.5V$			-1.3	mA
		$V_{DD}=15V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=13.5V$			-3.4	mA
Low-Level Output Current	I_{OL}	$V_{DD}=5V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=0.4V$	0.51			mA
		$V_{DD}=10V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=0.5V$	1.3			mA
		$V_{DD}=15V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=1.5V$	3.4			mA
Input Leakage Current	$I_{I(LEAK)}$	$V_{DD}=15V, V_{IN}=0V$ or V_{DD}			± 0.1	μA
3-State Output Leakage Current	I_{OUT}	$V_{DD}=15V, V_{IN}=0V$ or $V_{DD}, V_{OUT}=0V$ or V_{DD}			± 0.4	μA
Quiescent Supply Current	I_{DD}	$V_{DD}=5V, V_{IN}=0V$ or V_{DD}			5	μA
		$V_{DD}=10V, V_{IN}=0V$ or V_{DD}			10	μA
		$V_{DD}=15V, V_{IN}=0V$ or V_{DD}			20	μA

Note: I_{OL} and I_{OH} are tested one output at a time.

■ SWITCHING CHARACTERISTICS

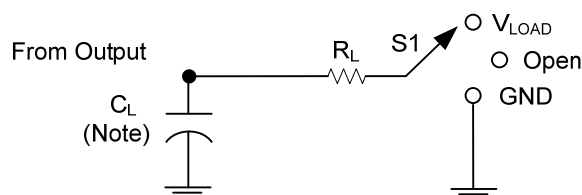
(Input: $t_R=t_F=20\text{ns}$, $C_L=50\text{pF}$, $R_L=200\text{K}\Omega$, $T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (CP) to Output (QS1)	t_{PHL}/t_{PLH}	$V_{DD}=5\text{V}$			600	ns
		$V_{DD}=10\text{V}$			250	ns
		$V_{DD}=15\text{V}$			190	ns
Propagation Delay From Input (CP) to Output (QS2)	t_{PHL}/t_{PLH}	$V_{DD}=5\text{V}$			460	ns
		$V_{DD}=10\text{V}$			220	ns
		$V_{DD}=15\text{V}$			150	ns
Propagation Delay From Input (CP) to Output (QPn)	t_{PHL}/t_{PLH}	$V_{DD}=5\text{V}$			840	ns
		$V_{DD}=10\text{V}$			390	ns
		$V_{DD}=15\text{V}$			270	ns
Propagation Delay From Input (STR) to Output (QPn)	t_{PHL}/t_{PLH}	$V_{DD}=5\text{V}$			580	ns
		$V_{DD}=10\text{V}$			290	ns
		$V_{DD}=15\text{V}$			200	ns
Propagation Delay From Input (OE) to Output (QPn)	t_{PHZ}/t_{PZH}	$V_{DD}=5\text{V}$			280	ns
		$V_{DD}=10\text{V}$			120	ns
		$V_{DD}=15\text{V}$			90	ns
Propagation Delay From Input (OE) to Output (QPn)	t_{PLZ}/t_{PZL}	$V_{DD}=5\text{V}$			200	ns
		$V_{DD}=10\text{V}$			100	ns
		$V_{DD}=15\text{V}$			80	ns
Output Transition Time	t_{THL}/t_{TLH}	$V_{DD}=5\text{V}$			200	ns
		$V_{DD}=10\text{V}$			100	ns
		$V_{DD}=15\text{V}$			80	ns
Maximum Clock Input Frequency	f_{CL}	$V_{DD}=5\text{V}$	1.25			MHz
		$V_{DD}=10\text{V}$	2.5			MHz
		$V_{DD}=15\text{V}$	3			MHz
Minimum Clock Pulse Width	t_w	$V_{DD}=5\text{V}$	200			ns
		$V_{DD}=10\text{V}$	100			ns
		$V_{DD}=15\text{V}$	80			ns
Minimum Strobe Pulse Width	t_w	$V_{DD}=5\text{V}$	200			ns
		$V_{DD}=10\text{V}$	80			ns
		$V_{DD}=15\text{V}$	70			ns
Minimum Data Setup Time	t_{SU}	$V_{DD}=5\text{V}$	125			ns
		$V_{DD}=10\text{V}$	55			ns
		$V_{DD}=15\text{V}$	35			ns

■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

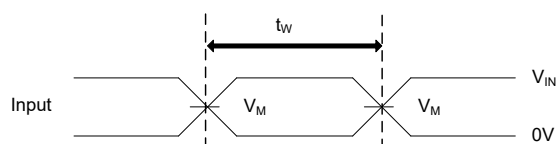
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	Any Input			7.5	pF

■ TEST CIRCUIT AND WAVEFORMS

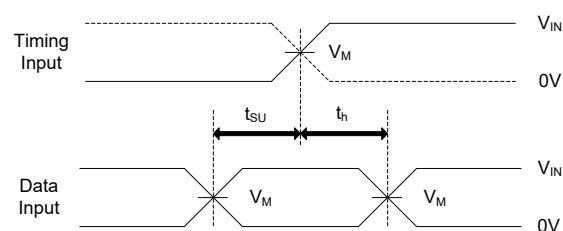


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

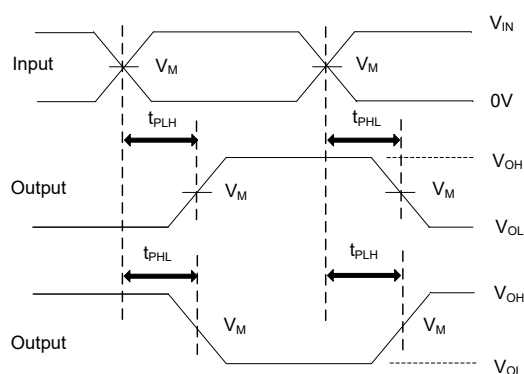
V_{DD}	Inputs		V_M	V_{LOAD}	C_L	R_L
	V_{IN}	t_R / t_F				
5V ~ 15V	0 or V_{DD}	$\leq 20\text{ns}$	$0.5 \times V_{DD}$	V_{DD}	50pF	200K Ω



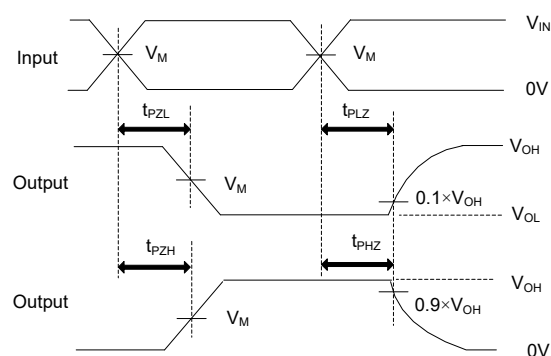
PULSE WIDTH



SETUP TIME AND HOLD TIME



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 10\text{MHz}$, $Z_0 = 50\Omega$.

■ TEST CIRCUIT AND WAVEFORMS (Cont.)

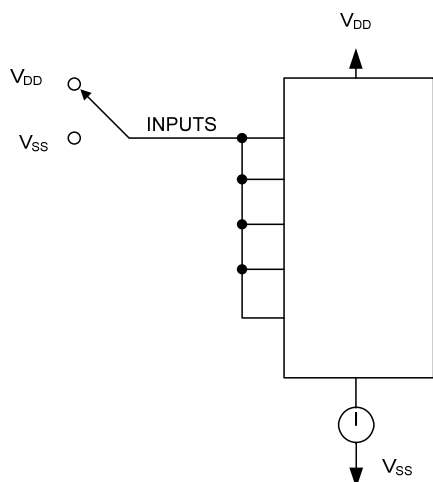


Fig. 1 Quiescent device current test circuit

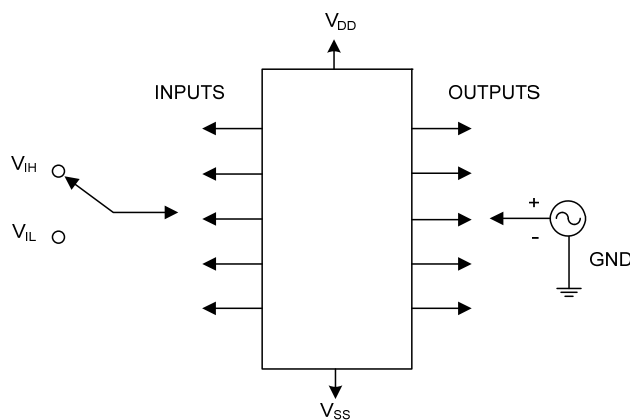


Fig. 2 Input voltage test circuit

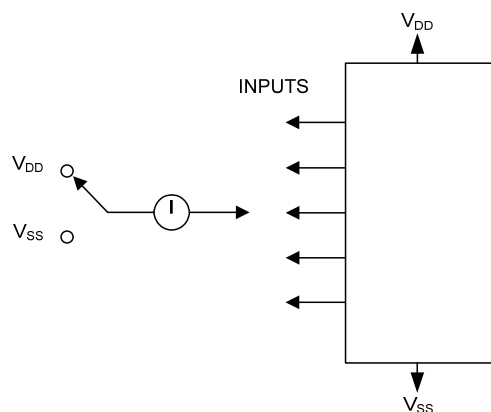


Fig. 3 Input current test circuit

Note: Measure inputs sequentially, to both V_{DD} and V_{SS} ; Connect all unused inputs to either V_{DD} or V_{SS} .

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