



U74LVC3G04

CMOS IC

TRIPLE INVERTER GATE

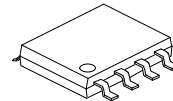
DESCRIPTION

The **U74LVC3G04** is a triple inverter gate which provides the Boolean function $Y = \overline{A}$.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FEATURES

- * Wide supply voltage range from 1.65V to 5.5V
- * Inputs accept voltages up to 5.5V
- * I_{OFF} supports partial-power-down mode
- * Low static power consumption; $I_{CC}=10\mu A$ (Max.)



SOP-8



MSOP-8



CDFN2030-8

ORDERING INFORMATION

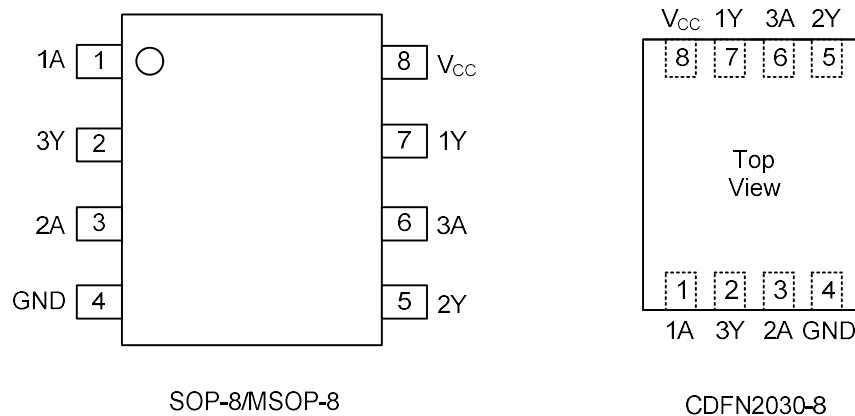
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC3G04L-S08-R	U74LVC3G04G-S08-R	SOP-8	Tape Reel
U74LVC3G04L-SM1-R	U74LVC3G04G-SM1-R	MSOP-8	Tape Reel
U74LVC3G04L-CK08-2030-R	U74LVC3G04G-CK08-2030-R	CDFN2030-8	Tape Reel

U74LVC3G04G-S08-R	(1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) S08: SOP-8, SM1: MSOP-8, CK08-2030: CDFN2030-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

SOP-8 / MSOP-8	CDFN2030-8
UTC □ □ □ □ → Date Code LVC3G04 □ → L: Lead Free □ → G: Halogen Free □ □ □ □ → Lot Code	LVC 3G04 • □ □ □ → Date Code

PIN CONFIGURATION



FUNCTION TABLE

INPUT(A)	OUTPUT(Y)
H	L
L	H

Note: H: High voltage level; L: Low voltage level

LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +6.5	V
Input Voltage	V_{IN}		-0.5 ~ +6.5	V
Output Voltage	V_{OUT}	Output in the high or low state	-0.5 ~ $V_{CC} + 0.5$	V
		Output in the power-off state	-0.5 ~ +6.5	V
Continuous V_{CC} or GND Current	I_{CC}		±100	mA
Continuous Output Current	I_{OUT}	$V_{OUT}=0V \sim V_{CC}$	±50	mA
Input Clamp Current	I_{IK}	$V_{IN}<0V$	-50	mA
Output Clamp Current	I_{OK}	$V_{OUT}>V_{CC}$ or $V_{OUT}<0V$	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=1.8V\pm0.15V, 2.5V\pm0.2V$			20	ns/V
		$V_{CC}=3.3V\pm0.3V$			10	ns/V
		$V_{CC}=5V\pm0.5V$			5	ns/V
Operating Temperature	T_A		-40		+125	°C

Note: This condition is only determined from design. It can't be 100% tested in mass production.

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	$V_{CC}=1.8\pm0.15V$	$0.65\times V_{CC}$			V
		$V_{CC}=2.5\pm0.2V$	1.7			V
		$V_{CC}=3.3\pm0.3V$	2			V
		$V_{CC}=5\pm0.5V$	$0.7\times V_{CC}$			V
Low-level Input Voltage	V_{IL}	$V_{CC}=1.8\pm0.15V$			$0.35\times V_{CC}$	V
		$V_{CC}=2.5\pm0.2V$			0.7	V
		$V_{CC}=3.3\pm0.3V$			0.8	V
		$V_{CC}=5\pm0.5V$			$0.3\times V_{CC}$	V
High-Level Output Voltage	V_{OH}	$V_{CC}=1.65 \sim 5.5V, I_{OH}=-100\mu A$	$V_{CC}-0.1$			V
		$V_{CC}=1.65V, I_{OH}=-4mA$	1.2			V
		$V_{CC}=2.3V, I_{OH}=-8mA$	1.9			V
		$V_{CC}=3.0V, I_{OH}=-16mA$	2.4			V
		$V_{CC}=3.0V, I_{OH}=-24mA$	2.3			V
		$V_{CC}=4.5V, I_{OH}=-32mA$	3.8			V
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65 \sim 5.5V, I_{OL}=100\mu A$			0.1	V
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	V
		$V_{CC}=2.3V, I_{OL}=8mA$			0.3	V
		$V_{CC}=3.0V, I_{OL}=16mA$			0.4	V
		$V_{CC}=3.0V, I_{OL}=24mA$			0.55	V
		$V_{CC}=4.5V, I_{OL}=32mA$			0.55	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0 \sim 5.5V$, $V_{IN}=5.5V$ or GND			± 5	μA
Power OFF Leakage Current	I_{off}	$V_{CC}=0V$, V_{IN} or $V_{OUT}=5.5V$			± 10	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=1.65 \sim 5.5V$, $V_{IN}=V_{CC}$ or GND, $I_{OUT}=0A$			10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=3 \sim 5.5V$, One input at $V_{CC}-0.6V$, Other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_I	$V_{CC}=3.3V$, $V_{IN}=V_{CC}$ or GND		3.5		pF

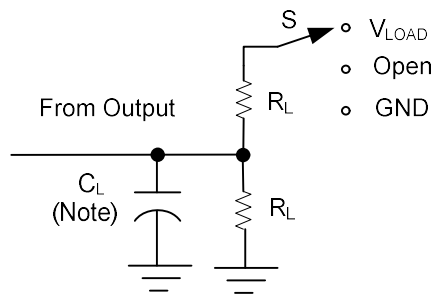
■ SWITCHING CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PD}	$V_{CC}=1.8\pm 0.15V$, $C_L=30pF$, $R_L=1k\Omega$	3.2		7.9	ns
		$V_{CC}=2.5\pm 0.2V$, $C_L=30pF$, $R_L=500\Omega$	1.5		4.4	ns
		$V_{CC}=3.3\pm 0.3V$, $C_L=50pF$, $R_L=500\Omega$	1.4		4.1	ns
		$V_{CC}=5\pm 0.5V$, $C_L=50pF$, $R_L=500\Omega$	1.1		3.2	ns

■ OPERATING CHARACTERISTICS ($f=10MHz$, $T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC}=1.8V$		16		pF
		$V_{CC}=2.5V$		16		pF
		$V_{CC}=3.3V$		16		pF
		$V_{CC}=5V$		18		pF

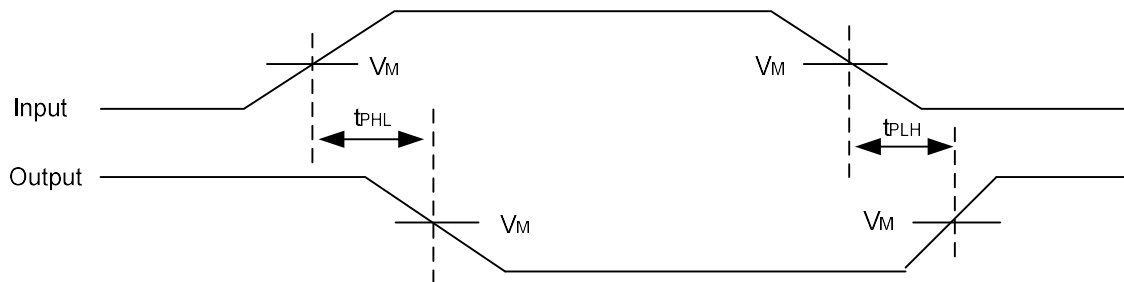
■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

Note: C_L includes probe and jig capacitance.

V_{CC}	V_{IN}	t_R / t_F	V_M	C_L	R_L	V_{Δ}
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	1K Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	500 Ω	0.15V
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	50pF	500 Ω	0.3V
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	50pF	500 Ω	0.3V



Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_O = 50\Omega$.

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