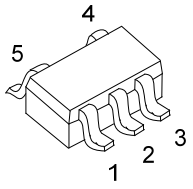
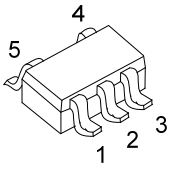
U74LVC1G79

CMOS IC

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



SOT-23-5



SOT-353

■ DESCRIPTION

The **U74LVC1G79** is a single positive-edge-triggered D-type flip-flop.

When data at the data input (D) meets the set-up time requirements, the data is transferred to the outputs (Q) on the positive-going edge of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the outputs.

This device has power-down protective circuit, preventing device destruction when it is powered down.

■ FEATURES

* Operate from 1.65V to 5.5V
* Inputs accept voltages to 5.5V
* I_{off} supports partial-power-down mode
* Low power dissipation: I_{CC}=10μA (Max.)
* ±24mA output drive(V_{CC}=3.3V)

■ ORDERING INFORMATION

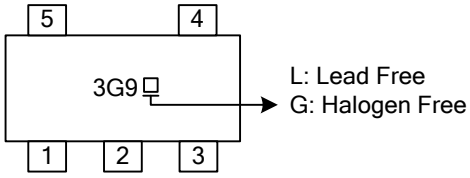
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC1G79G-AE5-R	U74LVC1G79G-AE5-R	SOT-23-5	Tape Reel
U74LVC1G79G-AL5-R	U74LVC1G79G-AL5-R	SOT-353	Tape Reel

U74LVC1G79G-AE5-R

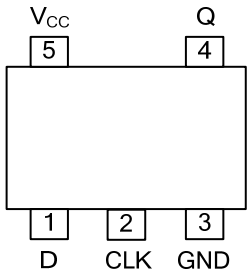
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) AE5: SOT-23-5, AL5: SOT-353
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

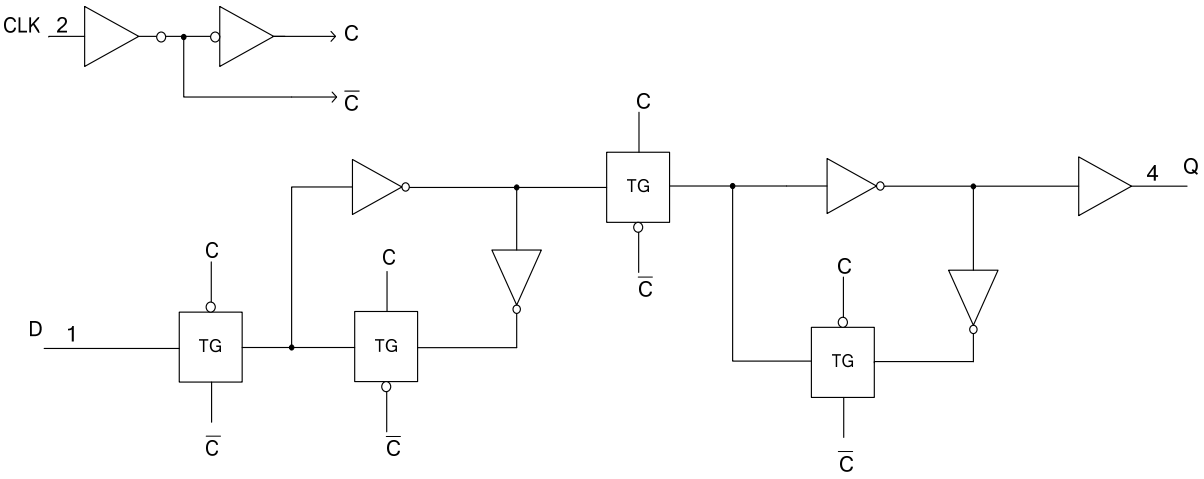


■ FUNCTION TABLE (EACH GATE)

INPUT		OUTPUT
CLK	D	Q
↑	H	H
↑	L	L
L	X	Q_0

Note: H: HIGH voltage level; L: LOW voltage level; X: Don't care; ↑: Low to High CLK transition
Q_0: indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CLK transition

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5 ~ +6.5	V
Input Voltage		V_{IN}	-0.5 ~ +6.5	V
Output Voltage	Output in the high or low state	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
	Output in the high-impedance or power-off state		-0.5 ~ +6.5	V
V_{CC} or GND Current		I_{CC}	±100	mA
Continuous Output Current (V_{OUT}=0 ~ V_{CC})		I_{OUT}	±50	mA
Input Clamp Current (V_{IN}<0)		I_{IK}	-50	mA
Output Clamp Current (V_{OUT}<0)		I_{OK}	-50	mA
Storage Temperature Range		T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
High-Level Input Voltage	V_{IH}	V_{CC}=1.65V~1.95V	0.65xV_{CC}			V
		V_{CC}=2.3V~2.7V	1.7			
		V_{CC}=3.0V~3.6V	2			
		V_{CC}=4.5V~5.5V	0.7xV_{CC}			
Low-Level Input Voltage	V_{IL}	V_{CC}=1.65V~1.95V			0.35xV_{CC}	V
		V_{CC}=2.3V~2.7V			0.7	
		V_{CC}=3.0V~3.6V			0.8	
		V_{CC}=4.5V~5.5V			0.3xV_{CC}	
High-level Output Current	I_{OH}	V_{CC}=1.65V			-4	mA
		V_{CC}=2.3V			-8	mA
		V_{CC}=3.0V			-16	mA
		V_{CC}=3.0V			-24	mA
		V_{CC}=4.5V			-32	mA
Low-level Output Current	I_{OL}	V_{CC}=1.65V			4	mA
		V_{CC}=2.3V			8	mA
		V_{CC}=3.0V			16	mA
		V_{CC}=3.0V			24	mA
		V_{CC}=4.5V			32	mA
Input Transition Rise or Fall Rate	Δt/Δv	V_{CC}=1.65V~1.95V, 2.3V~2.7V			20	ns/V
		V_{CC}=3.0V~3.6V			10	ns/V
		V_{CC}=4.5V~5.5V			5	ns/V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	V_{CC}=1.65V~5.5V, I_{OH}=-100μA	V_{CC}-0.1			V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2			
		V_{CC}=2.3V, I_{OH}=-8mA	1.9			
		V_{CC}=3.0V, I_{OH}=-16mA	2.4			
		V_{CC}=3.0V, I_{OH}=-24mA	2.3			
		V_{CC}=4.5V, I_{OH}=-32mA	3.8			
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65V~5.5V, I_{OL}=-100μA			0.1	V
		V_{CC}=1.65V, I_{OL}=4mA			0.45	
		V_{CC}=2.3V, I_{OL}=8mA			0.3	
		V_{CC}=3.0V, I_{OL}=16mA			0.4	
		V_{CC}=3.0V, I_{OL}=24mA			0.55	
		V_{CC}=4.5V, I_{OL}=32mA			0.55	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0V~5.5V, V_{IN}=5.5V or GND			±10	μA
Power OFF Leakage Current	I_{OFF}	V_{CC}=0V, V_{IN} or V_{OUT}=5.5V			±10	μA
Quiescent Supply Current	I_Q	V_{CC}=1.65V ~ 5.5V, V_{IN}=5.5V or GND, I_{OUT}=0			10	μA
Additional Quiescent Supply Current	ΔI_Q	V_{CC} =3V~5.5V, One input at V_{CC}-0.6V, other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_{IN}	V_{CC}=3.3V, V_{IN}=V_{CC} or GND		4		pF

■ DYNAMIC CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	Conditions		MIN	TYP	MAX	UNIT
Clock frequency	f_{CLOCK}					160	MHZ
Pulse duration	t_w	V_{CC}=1.8V±0.15V		2.5			ns
		V_{CC}=2.5V±0.2V		2.5			
		V_{CC}=3.3V±0.3V		2.5			
		V_{CC}=5V±0.5V		2.5			
Setup time before CLK ↑	t_{su}	V_{CC}=1.8V±0.15V	Data in high	2.2			ns
		V_{CC}=2.5V±0.2V		1.4			
		V_{CC}=3.3V±0.3V		1.3			
		V_{CC}=5V±0.5V		1.2			
		V_{CC}=1.8V±0.15V	Data in low	2.6			
		V_{CC}=2.5V±0.2V		1.4			
		V_{CC}=3.3V±0.3V		1.3			
		V_{CC}=5V±0.5V		1.2			
Hold time ,data after CLK ↑	t_h	V_{CC}=1.8V±0.15V,		0.3			ns
		V_{CC}=2.5V±0.2V		0.4			
		V_{CC}=3.3V±0.3V		1			
		V_{CC}=5V±0.5V		0.5			

■ SWITCHING CHARACTERISTIC (Input: t_R, t_F≤2.5ns; PRR≤1MHz)

See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock pulse frequency	f_{MAX}	V_{CC} =1.65V~5.5V	160			MHz
Propagation delay from input (CLK) to output(Q)	t_{PLH}/t_{PHL}	V_{CC} =1.65V~1.95V,CL=15pF	2.5		9.1	ns
		V_{CC} =2.3V~2.7V,CL=15pF	1.2		6.0	
		V_{CC} =3.0V~3.6V,CL=15pF	1.0		4.0	
		V_{CC} =4.5V~5.5V,CL=15pF	0.8		3.8	
Propagation delay from input (CLK) to output(Q)	t_{PLH}/t_{PHL}	V_{CC} =1.65V~1.95V,CL=30pF	3.9		9.9	ns
		V_{CC} =2.3V~2.7V,CL=30pF	2.0		7.0	
		V_{CC} =3.0V~3.6V,CL=50pF	1.7		5.0	
		V_{CC} =4.5V~5.5V,CL=50pF	1.0		4.5	

■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	V_{CC}=3.3V, f=10MHz		27		pF

■ TEST CIRCUIT AND WAVEFORMS

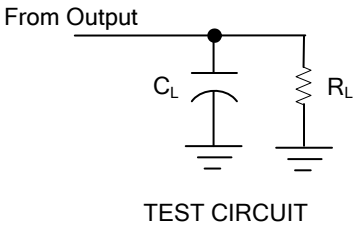


Fig.1 Load circuitry for switching times.

V_{CC}	V_{IN}	t_R,/t_F	V_M	C_L	R_L
1.8V±0.15V	V_{CC}	≤2ns	V_{CC}/2	15pF	1MΩ
				30pF	1KΩ
2.5V±0.2V	V_{CC}	≤2ns	V_{CC}/2	15pF	1MΩ
				30pF	500Ω
3.3V±0.3V	3 V	≤2.5ns	1.5V	15pF	1MΩ
				50pF	500Ω
5V±0.5V	V_{CC}	≤2.5ns	V_{CC}/2	15pF	1MΩ
				50pF	500Ω

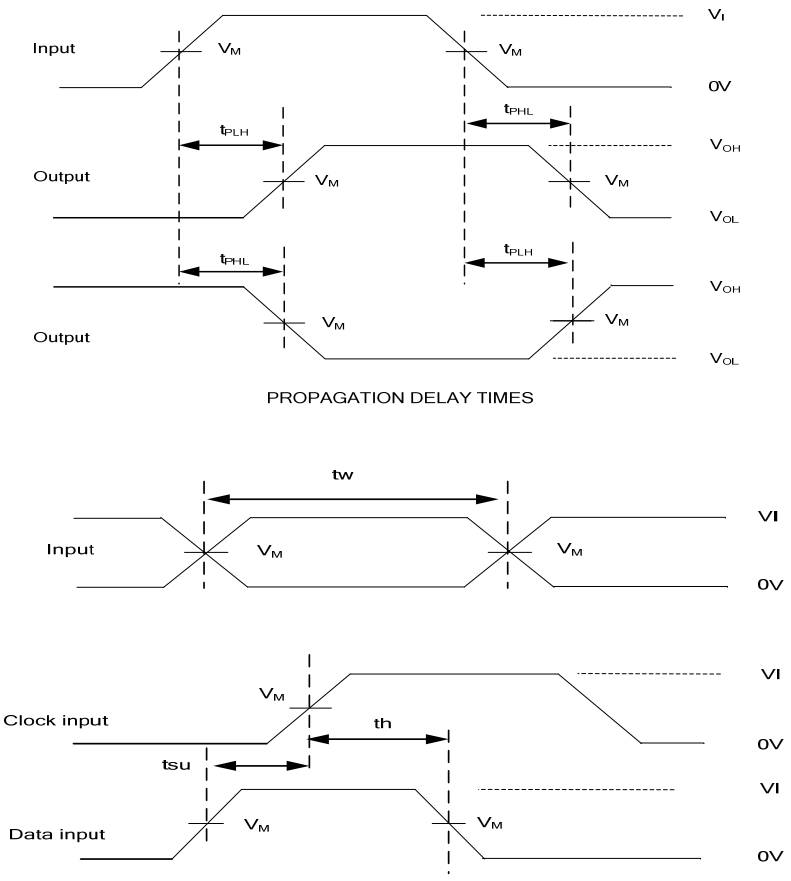


Fig. 2 Propagation delay from input to output and input voltage waveforms.

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Zo = 50Ω.