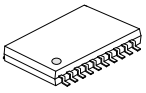
U74HCT540 **Preliminary** ***CMOS IC***

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



SOP-20

TSSOP-20

■ DESCRIPTION

The UTC **U74HCT540** contains octal buffers and line drivers. There are designed to have the performance of the 'HCT240 devices and a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

The 3-state control gate is a 2-input NOR. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state. The **U74HCT540** devices provide inverted data at the outputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

* Operation Voltage Range: 4.5V~5.5V
* Low Power Consumption, 80μA Max. I_{CC}
* Typical t_{pd} =12ns
* ±6mA Output Drive at 5V
* Low Input Current of 1μA Max
* Inputs Are TTL Voltage Compatible
* High-Current 3-State Outputs Interface Directly With System Bus or Can Drive Up To 15 LSTTL Loads
* Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT540L-S20-R	U74HCT540G-S20-R	SOP-20	Tape Reel
U74HCT540L-P20-R	U74HCT540G-P20-R	TSSOP-20	Tape Reel

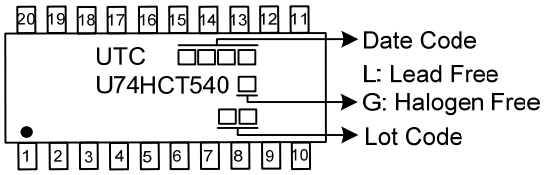
U74HCT540G-S20-R

(1)Packing Type — (1) R: Tape Reel

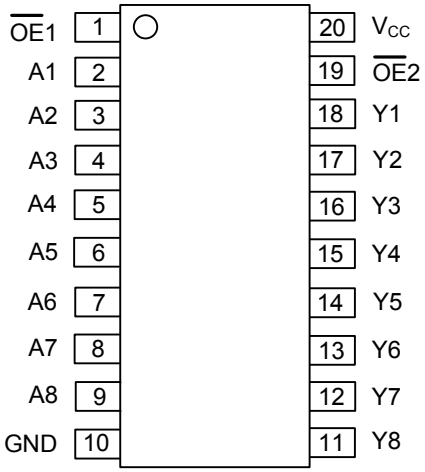
(2)Package Type — (2) S20: SOP-20, P20: TSSOP-20

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

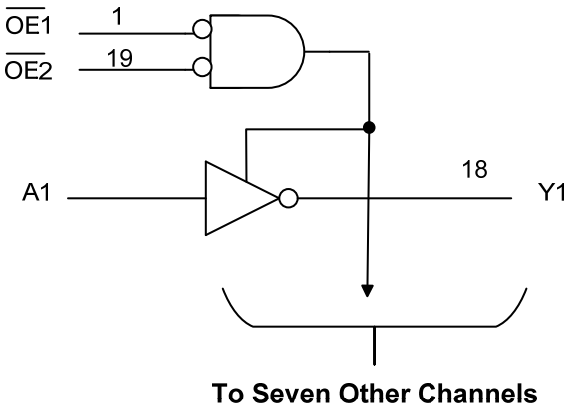


■ FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Note: H: HIGH voltage level. ; L: LOW voltage level. ; X: Don't care. ; Z: High impedance OFF-state.

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})	I_{IK}	±20	mA
Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})	I_{OK}	±20	mA
Output Current (V_{OUT} = 0 or V_{CC})	I_{OUT}	±35	mA
V_{CC} or GND Current	I_{CC}	±70	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4.5	5	5.5	V
Input Voltage	V_{IN}	0		V_{CC}	V
Output Voltage	V_{OUT}	0		V_{CC}	V
Input Transition Rise or Fall Rate	t_T			500	ns
Operating Temperature	T_{OPR}	-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC}=4.5V~5.5V	2.0			V
Low-Level Input Voltage	V_{IL}	V_{CC}=4.5V~5.5V			0.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=-20μA	4.4	4.499		V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OH}=-6mA	3.98	4.3		V
Low-Level Output Voltage	V_{OL}	V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=4.5V, V_{IN}=V_{IH} or V_{IL}, I_{OL}=6mA		0.17	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}=V_{CC} or GND		±0.1	±100	nA
Output OFF -State Current	I_{OZ}	V_{CC}=5.5V, V_{OUT}=V_{CC} or GND V_{IN}=V_{IH} or V_{IL}		±0.01	±0.5	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8	μA
Additional Quiescent Supply Current	$\triangle I_{CC}$	V_{CC}=5.5V,One input at 0.5V or 2.4V, other inputs at 0 or V_{CC}		1.4	2.4	mA
Input Capacitance	C_{IN}	V_{CC}=4.5V~5.5V		3	10	pF

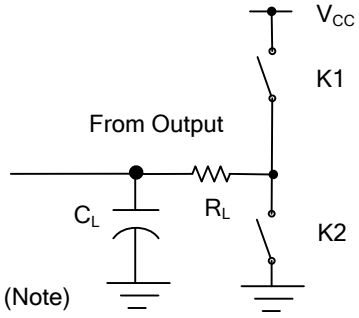
■ DYNAMIC CHARACTERISTICS (R_L=1kΩ, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (A) to Output (Y)	t_{PD}	V_{CC}=4.5V	C_L=50pF		13	20	ns
		V_{CC}=5.5V			12	18	ns
		V_{CC}=4.5V	C_L=150pF		20	30	ns
		V_{CC}=5.5V			19	27	ns
3-State Output Enable Time From Input ($\overline{OE}$) to Output (Y)	t_{PZH}/t_{PZL}	V_{CC}=4.5V	C_L=50pF		20	30	ns
		V_{CC}=5.5V			18	27	ns
		V_{CC}=4.5V	C_L=150pF		26	40	ns
		V_{CC}=5.5V			25	36	ns
3-State Output Disable Time From Input ($\overline{OE}$) to Output (Y)	t_{PHZ}/t_{PLZ}	V_{CC}=4.5V	C_L=50pF		19	30	ns
		V_{CC}=5.5V			18	27	ns
Input Transition Rise And Fall Rate	t_R / t_F	V_{CC}=4.5V	C_L=50pF		8	12	ns
		V_{CC}=5.5V			7	11	ns
		V_{CC}=4.5V	C_L=150pF		17	42	ns
		V_{CC}=5.5V			14	38	ns

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	V_{CC}=4.5V~5.5V		3	10	pF
Power Dissipation Capacitance	C_{PD}	No Load		50		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

Note： C_L includes probe and jig capacitance.