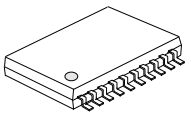
U74CBTLV3245

CMOS IC

LOW-VOLTAGE OCTAL FET BUS SWITCH



TSSOP-20

■ DESCRIPTION

The **U74CBTLV3245** provides eight bits of high-speed bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch. When output enable ($\overline{OE}$) is low, the 8-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

* 5Ω Switch Connection Between Two Ports
* Standard '245-Type Pinout
* Isolation Under Power-Off Conditions
* Rail-to-Rail Switching on Data I/O Ports
* I_{OFF} Supports Partial-Power-Down Mode Operation

■ ORDERING INFORMATION

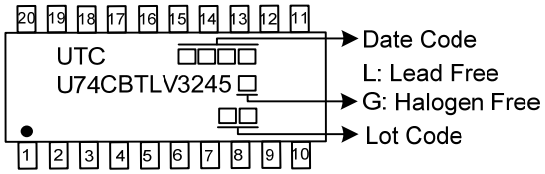
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBTLV3245L-P20-R	U74CBTLV3245G-P20-R	TSSOP-20	Tape Reel

U74CBTLV3245G-P20-R

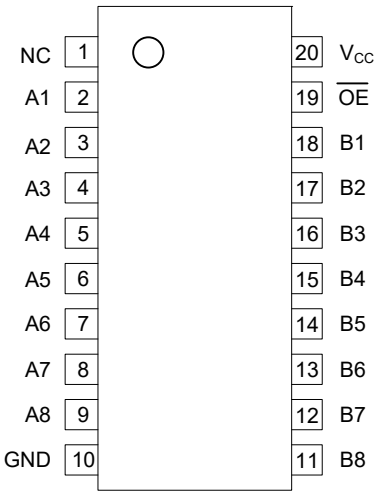
(1)Packing Type
(2) Package Type
(3) Green Package

(1) R: Tape Reel
(2) P20: TSSOP-20
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



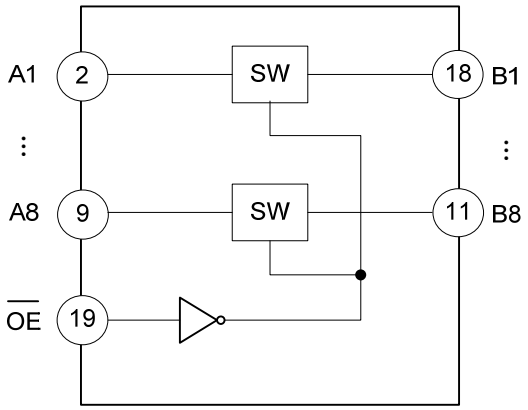
■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	NC		No connection
2-9	An	I/O	Input/output An
10	GND		Ground
11 ~18	Bn	I/O	Input/output Bn
19	$\overline{OE}$	I	Pull $\overline{OE}$ low, An=Bn
20	V_{CC}		Supply Voltage 1.65V ≤ V_{CCB} ≤ 5.5V

■ FUNCTION TABLE (each bus switch)

INPUT ($\overline{OE}$)	FUNCTION
L	A port = B port
H	Disconnect

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 4.6	V
Input Voltage (Note 2)	V_I	-0.5 ~ 4.6	V
Continuous channel current		128	mA
Input Clamp Current ($V_{I/O}$<0)	I_{IK}	-50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.3		3.6	V
High-control input voltage	V_{IH}	V_{CC}=2.3V~2.7V	1.7			V
		V_{CC}=2.7V~3.6V	2			V
Low-control input voltage	V_{IL}	V_{CC}=2.3V~2.7V			0.7	V
		V_{CC}=2.7V~3.6V			0.8	V
Operating Temperature	T_A		-40		+85	°C

Note: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ STATIC CHARACTERISTICS

PARAMETER		SYMBOL	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
Digital Input Diode Voltage	Control Inputs	V_{IK}	V_{CC} =3V, I_I=-18mA					-1.2	V
	Data Inputs							-0.8	V
Input Leakage Current		I_I	V_{CC}=3.6V, V_I=V_{CC} or GND					±60	μA
Power off Leakage Current		I_{OFF}	V_{CC}=0, V_I or V_O=0 to 3.6V					40	μA
Quiosceut Supply Current		I_{CC}	V_{CC}=3.6V, V_I= V_{CC} or GND, I_O=0					20	μA
Additional Quiescent Supply Current (Note 2)	Control Inputs	ΔI_{CC}	V_{CC}=3.6V, One input at 3V, Other inputs at V_{CC} or GND					300	μA
Control input Capacitance	Control Inputs	C_I	V_O=3V or 0				4		pF
I/O Capacitance OFF		$C_{IO(OFF)}$	V_O=3V or 0, $\overline{OE}$ =V_{CC}				9		pF
Resistor between two ports (Note 3)		R_{ON}	V_{CC}=2.3V Typ. at V_{CC}=2.5V	V_I=0	I_O=64mA		5	8	Ω
					I_O=24mA		5	8	Ω
				V_I=1.7V, I_O=-15mA			27	40	Ω
			V_{CC}=3V	V_I=0V	I_O=64mA		5	7	Ω
					I_O=24mA		5	7	Ω
				V_I=2.4V, I_O=-15mA			10	15	Ω

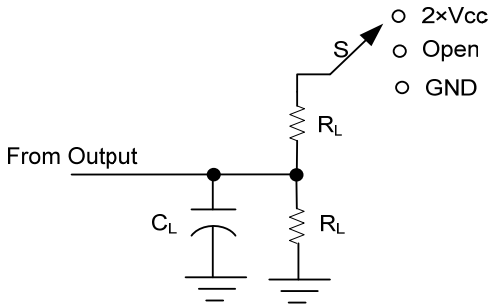
Notes: 1. All typical values are at V_{CC}=3.3V, T_A=25°C, unless otherwise Specified.
2. This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
3. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

■ DYNAMIC CHARACTERISTICS

Over recommended operating free-air temperature range, unless otherwise specified. (See Figure. 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From input (A or B) to output (B or A)	t_{pd} (t_{PLH}/t_{PHL})	V_{CC}=2.5V±0.2V			0.15	ns
		V_{CC}=3.3V±0.3V			0.25	ns
From input ($\overline{OE}$) to output (A or B)	t_{en} (t_{PZL}/t_{PZH})	V_{CC}=2.5V±0.2V	1.0		6.0	ns
		V_{CC}=3.3V±0.3V	1.0		4.7	ns
From input ($\overline{OE}$) to output (A or B)	t_{dis} (t_{PLZ}/t_{PHZ})	V_{CC}=2.5V±0.2V	1.0		6.1	ns
		V_{CC}=3.3V±0.3V	1.0		6.4	ns

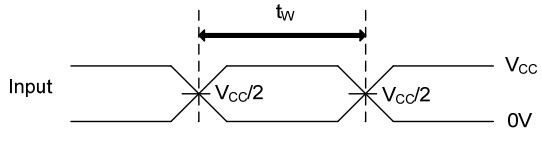
■ TEST CIRCUIT AND WAVEFORMS



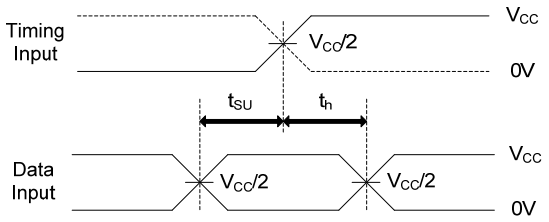
V_{CC}	C_L	R_L	V_Δ
2.5V±0.2V	30pF	500Ω	0.15V
3.3V±0.3V	50pF	500Ω	0.3V

TEST	S
t_{PD}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	2×Vcc

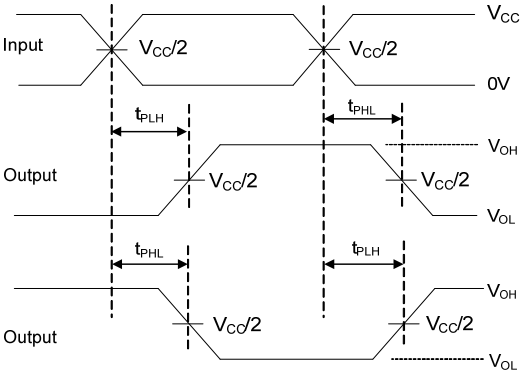
Note: C_L includes probe and jig capacitance.
t_{PLZ} and t_{PHZ} are the same as t_{dis}.
t_{PZL} and t_{PZH} are the same as t_{en}.
t_{PLH} and t_{PHL} are the same as t_{PD}.



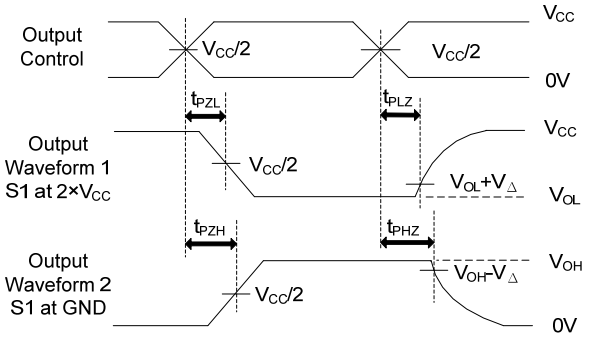
PULSE DURATION



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Note: All input pulses are supplied by generators having the following characteristics:
t_r, $t_f \le$ 2ns; $P_{RR} \le$ 10MHz; Z_O=50Ω.

Figure. 1 Load circuitry and voltage waveforms