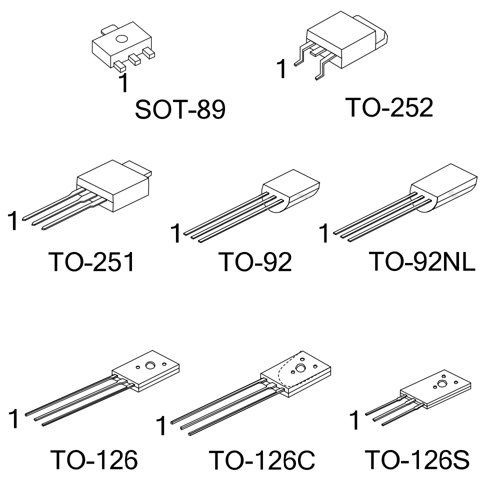
MJE13003-P

NPN SILICON TRANSISTOR

NPN SILICON POWER TRANSISTOR



■ DESCRIPTION

These devices are designed for high-voltage and high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220V applications in switch mode.

■ FEATURES

* Reverse biased SOA with inductive load @ Tc=100°C
* Inductive switching matrix 0.5 ~ 1.5 Amp, 25 and 100°C
  Typical tc = 290ns @ 1A, 100°C.
* 700V blocking capability

■ APPLICATIONS

* Switching regulator's, inverters
* Motor controls
* Solenoid/relay drivers
* Deflection circuits

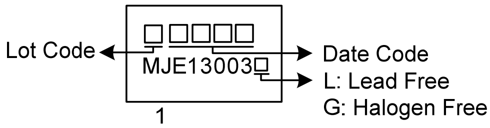
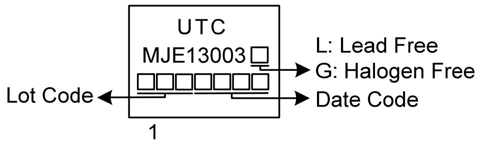
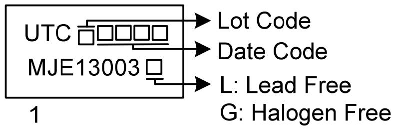
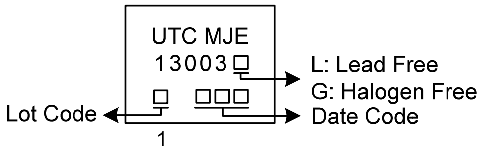
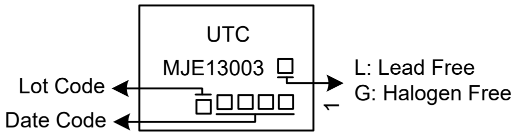
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen-Free		1	2	3	
MJE13003L-P-AB3-R	MJE13003G-P-AB3-R	SOT-89	B	C	E	Tape Reel
MJE13003L-P-T60-K	MJE13003G-P-T60-K	TO-126	B	C	E	Bulk
MJE13003L-P-T6C-A-K	MJE13003G-P-T6C-A-K	TO-126C	E	C	B	Bulk
MJE13003L-P-T6C-F-K	MJE13003G-P-T6C-F-K	TO-126C	B	C	E	Bulk
MJE13003L-P-T6S-K	MJE13003G-P-T6S-K	TO-126S	B	C	E	Bulk
MJE13003L-P-T92-B	MJE13003G-P-T92-B	TO-92	E	C	B	Tape Box
MJE13003L-P-T92-K	MJE13003G-P-T92-K	TO-92	E	C	B	Bulk
MJE13003L-P-T92-R	MJE13003G-P-T92-R	TO-92	E	C	B	Tape Reel
MJE13003L-P-T9N -B	MJE13003G-P-T9N-B	TO-92NL	E	C	B	Tape Box
MJE13003L-P-T9N -K	MJE13003G-P-T9N-K	TO-92NL	E	C	B	Bulk
MJE13003L-P-T9N -R	MJE13003G-P-T9N-R	TO-92NL	E	C	B	Tape Reel
MJE13003L-P-TM3-T	MJE13003G-P-TM3-T	TO-251	B	C	E	Tube
MJE13003L-P-TN3-R	MJE13003G-P-TN3-R	TO-252	B	C	E	Tape Reel

Note: Pin assignment: B: Base C: Collector E: Emitter

MJE13003G-P-T6C-A-K (1)Packing Type (2)Pin Assignment (3)Package Type (4)Green Package	(1) R: Tape Reel, K: Bulk, B: Tape Box, T: Tube (2) refer to Pin Assignment (for TO-126C) (3) T60: TO-126, T6C:TO-126C, T6S: TO-126S T92: TO-92, T9N: TO-92NL, TM3: TO-251, TN3: TO-252 (4) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

Package	MARKING
SOT-89	
TO-220 TO-251 TO-251S TO-252	
TO-126 TO-126C TO-126S	
TO-92	
TO-92NL	

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER			SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage			$V_{CEO(SUS)}$	400	V
Collector-Emitter Voltage (V_{BE}=0)			V_{CES}	700	V
Collector-Base Voltage			V_{CBO}	700	V
Emitter Base Voltage			V_{EBO}	9	V
Collector Current		Continuous	I_C	1.5	A
		Peak (1)	I_{CM}	3	
Base Current		Continuous	I_B	0.75	A
		Peak (1)	I_{BM}	1.5	
Emitter Current		Continuous	I_E	2.25	A
		Peak (1)	I_{EM}	4.5	
Total Power Dissipation	T_A=25°C	SOT-89	P_D	0.5	W
		TO-126/TO-126C TO-126S		1.4	W
		TO-92/TO-92NL		1.1	W
		TO-251/TO-252		1.56	W
	T_C=25°C	SOT-89		1.64	W
		TO-126/TO-126C TO-126S		20	W
		TO-92/TO-92NL		1.5	W
		TO-251/TO-252		25	W
Junction Temperature			T_J	+150	°C
Storage Temperature			T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS (Note)							
Collector-Emitter Sustaining Voltage		$V_{CEO(SUS)}$	I_C=10 mA , I_B=0	400			V
Collector Cutoff Current	T_C=25°C	I_{CEO}	V_{CEO}=Rated Value, $V_{BE(OFF)}$=1.5 V			1	mA
	T_C=100°C					5	mA
Emitter Cutoff Current		I_{EBO}	V_{EB}=9 V, I_C=0			1	mA
SECOND BREAKDOWN							
Second Breakdown Collector Current with bass forward biased		Is/b		See Fig.5			
Clamped Inductive SOA with base reverse biased		RB_{SOA}		See Fig.6			
ON CHARACTERISTICS (Note)							
DC Current Gain		h_{FE1}	I_C=0.4A, V_{CE}=5V	10		30	
		h_{FE2}	I_C=1A, V_{CE}=5V	5		30	
Collector-Emitter Saturation Voltage		$V_{CE(SAT)}$	I_C=0.5A, I_B=0.1A			0.5	V
			I_C=1A, I_B=0.25A			1	V
			I_C=1.2A, I_B=0.4A			3	V
			I_C=1A, I_B=0.25A, T_C=100°C			1	V
Base-Emitter Saturation Voltage		$V_{BE(SAT)}$	I_C=0.5A, I_B=0.1A			1	V
			I_C=1A, I_B=0.25A			1.2	V
			I_C=1A, I_B=0.25A, T_C=100°C			1.1	V
DYNAMIC CHARACTERISTICS							
Current-Gain-Bandwidth Product		f_T	I_C=100mA, V_{CE}=10V, f=1MHz	4	10		MHz
Output Capacitance		C_{OB}	V_{CB}=10V, I_E=0, f=0.1MHz		21		pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time		t_D	V_{CC}=125V, I_C=1A, I_{B1}=I_{B2}=0.2A, t_P=25μs, Duty Cycle≤1%		0.05	0.1	μs
Rise Time		t_R			0.5	1	μs
Storage Time		t_S			2	4	μs
Fall Time		t_F			0.4	0.7	μs
Inductive Load, Clamped (Table 1)							
Storage Time		t_{STG}	I_C=1A, Vclamp=300V, I_{B1}=0.2A, $V_{BE(OFF)}$=5Vdc, T_C=100°C		1.7	4	μs
Crossover Time		t_C			0.29	0.75	μs
Fall Time		t_F			0.15		μs

Note: Pulse Test : PW=300μs, Duty Cycle≤2%.

■ APPLICATION INFORMATION

Table 1.Test Conditions for Dynamic Performance

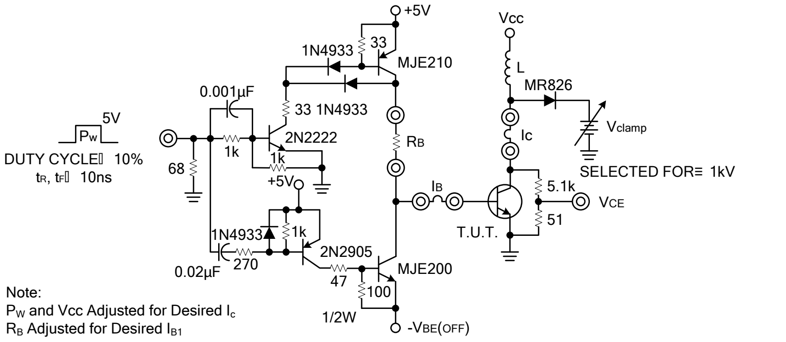
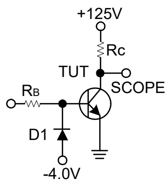
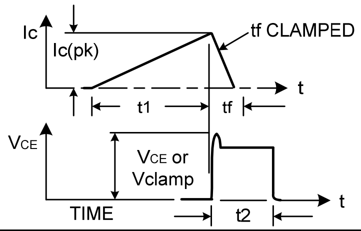
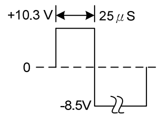
	Reverse Bias Safe Operating Area and Inductive Switching	Resistive Switching
Test Circuits		
Circuit Values	Coil Data : GAP for 30 mH/2 A V_{CC}=20V Ferroxcube core #6656 Lcoil=50mH Vclamp=300V Full Bobbin (~ 200 Turns) #20	V_{CC}=125V R_C=125Ω D1=1N5820 or Equiv. R_C=47Ω
Test Waveforms	Output Waveforms  t1 Adjusted to Obtain Ic $t_1 \approx \frac{Lcoil(Icpk)}{Vcc}$ $t_2 \approx \frac{Lcoil(Icpk)}{Vclamp}$ Test Equipment Scope-Tektronics 475 or Equivalent	 tr, tf<10ns Duty Cycly=1.0% RB and Rc adjusted for desired IB and Ic

Table 2. Typical Inductive Switching Performance

Ic (A)	Tc (°C)	t_{sv} (μs)	t_{RV} (μs)	t_{FI} (μs)	t_{TI} (μs)	tc (μs)
0.5	25 100	1.3 1.6	0.23 0.26	0.30 0.30	0.35 0.40	0.30 0.36
1	25 100	1.5 1.7	0.10 0.13	0.14 0.26	0.05 0.06	0.16 0.29
1.5	25 100	1.8 3	0.07 0.08	0.10 0.22	0.05 0.08	0.16 0.28

Note: All Data Recorded in the Inductive Switching Circuit in Table 1

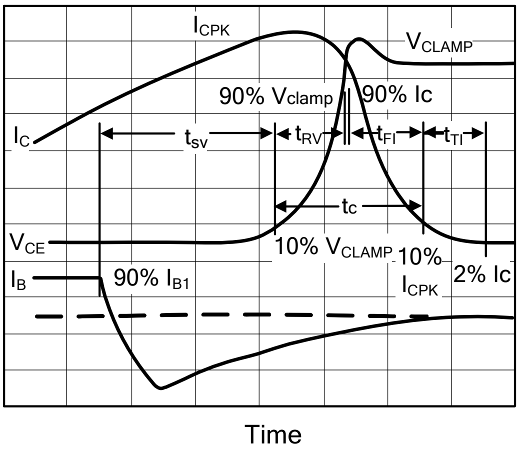


Fig.1 Inductive Switching Measurements

■ SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads, which are common to switch mode power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% Vclamp
t_{RV} = Voltage Rise Time, 10 ~ 90% Vclamp
t_{FI}= Current Fall Time, 90 ~ 10% I_C
t_{TI} = Current Tail, 10 ~ 2% I_C
t_C = Crossover Time, 10% Vclamp to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation:

$P_{SWT} = 1/2\ V_{CC} I_C\ (t_C)\ f$

In general, $t_{RV} + t_{FI} \approx t_C$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this transistor are the inductive switching speeds (t_C and t_{SV}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

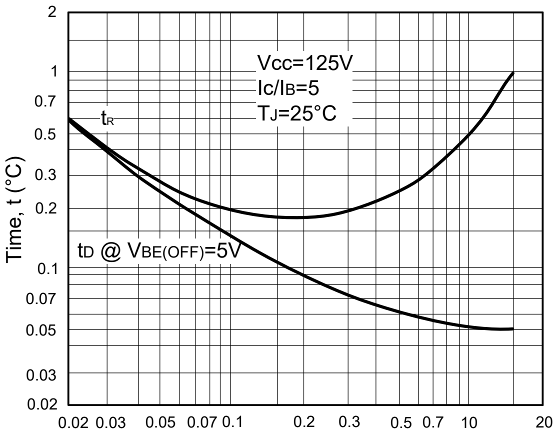


Fig.2 Turn-On Time

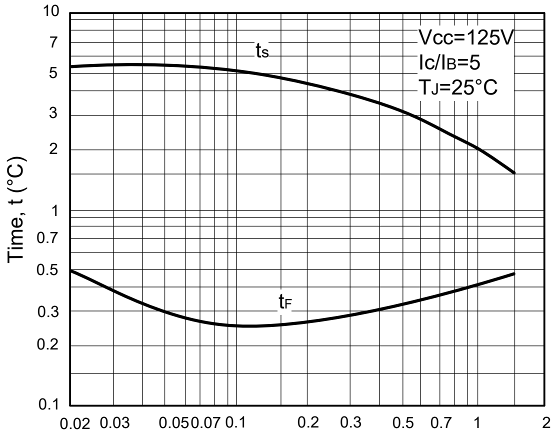


Fig.3 Turn-Off Time

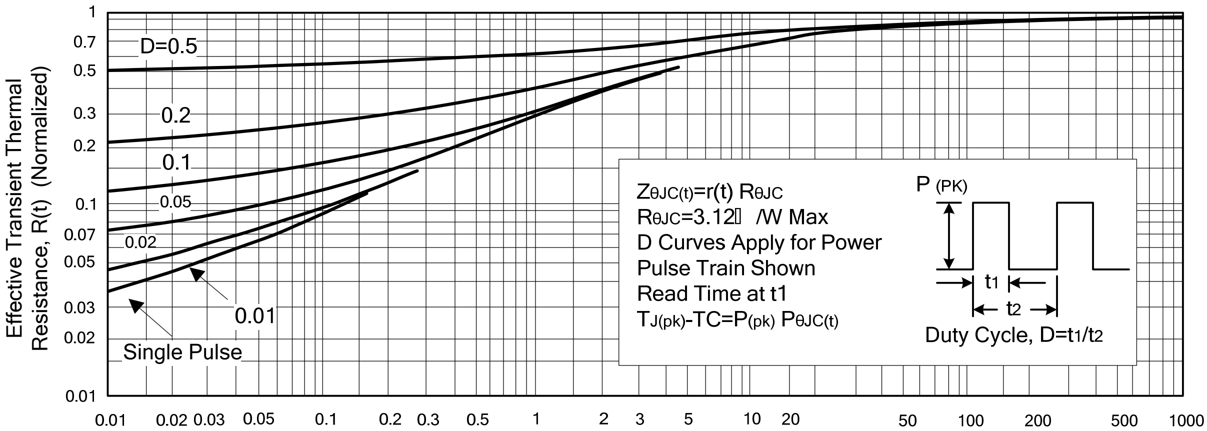


Fig.4 Thermal Response

■ SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig.5 is based on T_C = 25°C; $T_{J(PK)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Fig.5.

$T_{J(PK)}$ may be calculated from the data in Fig.4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as RB_{SOA}(Reverse Bias Safe Operating Area) and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Fig.6 gives RB_{SOA} characteristics.

The Safe Operating Area of Fig.5 and 6 are specified ratings (for these devices under the test conditions shown.)

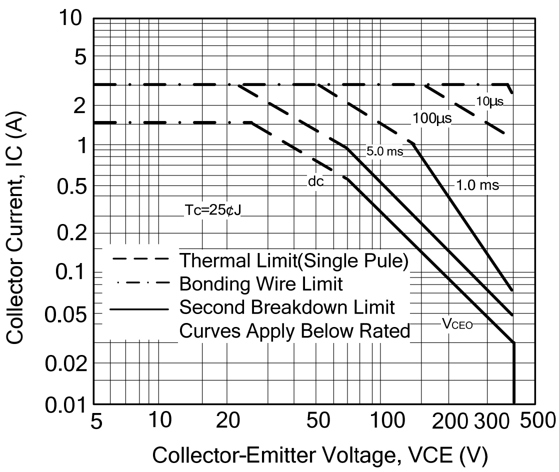


Fig.5 Active Region Safe Operating Area

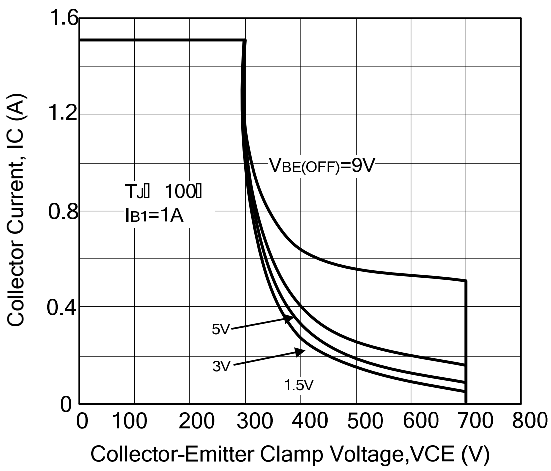
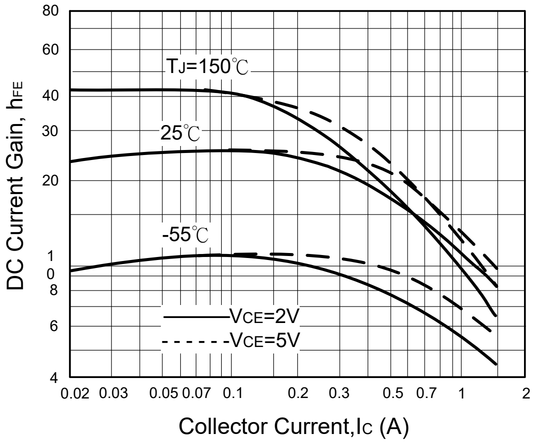


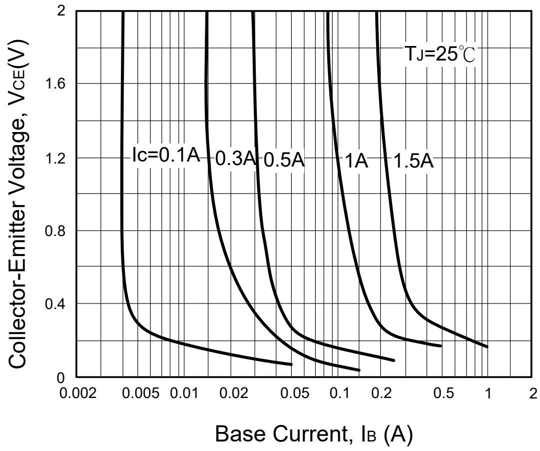
Fig.6 Reverse Bias Safe Operating Area

■ TYPICAL CHARACTERISTICS

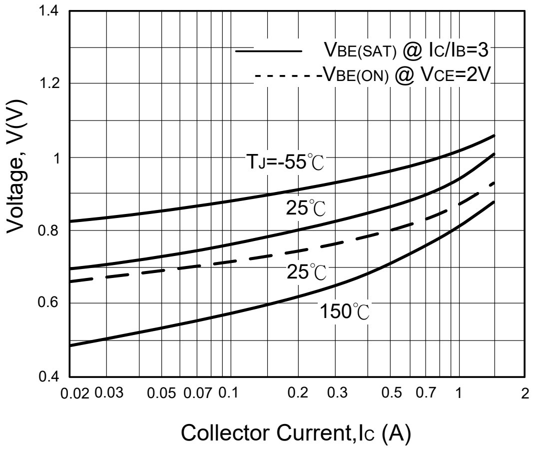
DC Current Gain



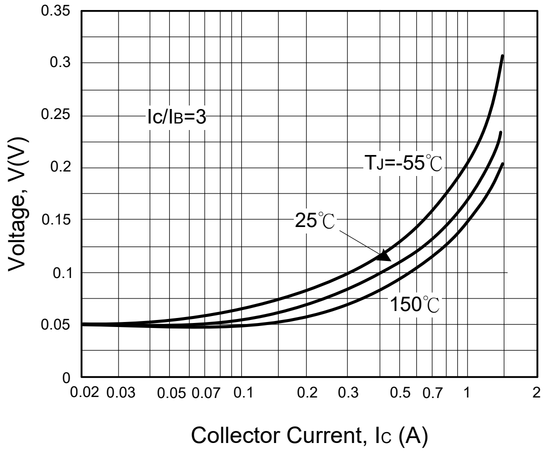
Collector Saturation Region



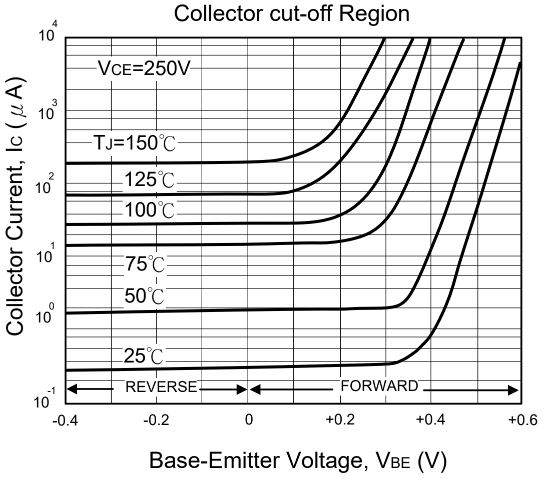
Base-Emitter Voltage



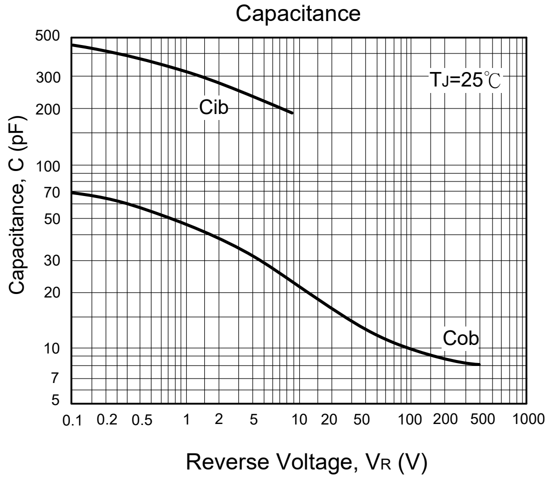
Collector-Emitter Saturation Region



Collector cut-off Region



Capacitance



■ TYPICAL CHARACTERISTICS(Cont.)

Forward Bias Power Derating