

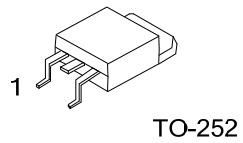
F4N60-ML1

Power MOSFET

**4.0A, 600V N-CHANNEL
POWER MOSFET**

■ DESCRIPTION

The UTC **F4N60-ML1** is a N-Channel enhancement mode silicon gate power MOSFET with Fast Body Diode, is designed high voltage, high speed power switching applications such, is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient AC to DC converters and bridge circuits.

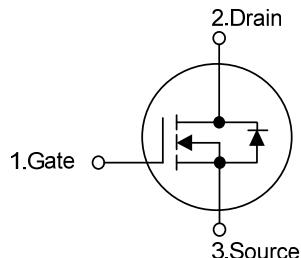


TO-252

■ FEATURES

- * $R_{DS(ON)} \leq 2.7 \Omega$ @ $V_{GS}=10V$, $I_D=2.0A$
- * Fast body diode MOSFET technology
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness

■ SYMBOL



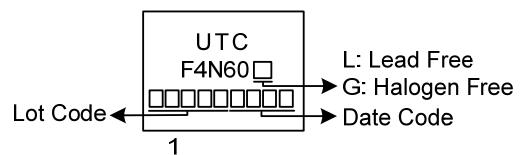
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
F4N60L-TN3-R	F4N60G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

F4N60G-TN3-R 	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



F4N60-ML1

Power MOSFET

■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	600	V
Gate-Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current	I_D	4	A
Pulsed Drain Current (Note 2)	I_{DM}	8	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	109 mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	7.6 V/ns	
Power Dissipation	P_D	50	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 30\text{mH}$, $I_{AS} = 2.7\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25 \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 4.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C/W}$
Junction to Case	θ_{JC}	2.5 (Note)	$^\circ\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

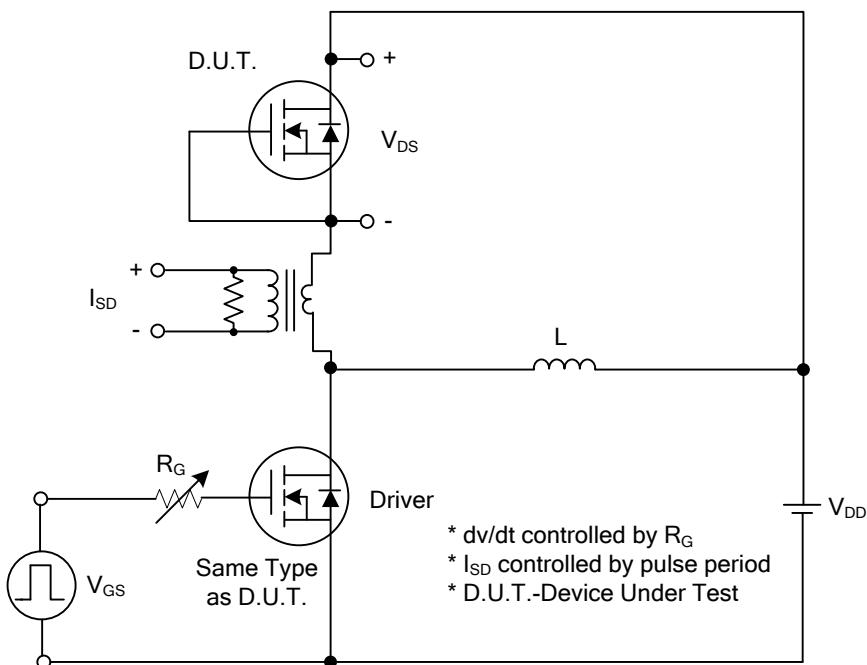
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	600			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate- Source Leakage Current	Forward	$V_{GS}=30\text{V}$, $V_{DS}=0\text{V}$			100	nA
	Reverse	$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=2.0\text{A}$			2.7	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$		550		pF
Output Capacitance	C_{OSS}			60		pF
Reverse Transfer Capacitance	C_{RSS}			5		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=480\text{V}$, $V_{GS}=10\text{V}$, $I_D=4\text{A}$ $I_G=1\text{mA}$ (Note 1, 2)		18		nC
Gate-Source Charge	Q_{GS}			6		nC
Gate-Drain Charge	Q_{GD}			4.2		nC
Turn-On Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=4\text{A}$, $R_G=25\Omega$ (Note 1, 2)		10		ns
Turn-On Rise Time	t_R			18		ns
Turn-Off Delay Time	$t_{D(OFF)}$			37		ns
Turn-Off Fall Time	t_F			26		ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Maximum Body-Diode Continuous Current	I_S				4	A
Maximum Body-Diode Pulsed Current	I_{SM}				8	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=4\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Reverse Recovery Time (Note 1)	t_{rr}	$I_S=4\text{A}$, $V_{GS}=0\text{V}$ $di/dt=100\text{A}/\mu\text{s}$		80		ns
Reverse Recovery Charge	Q_{rr}			141		nC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

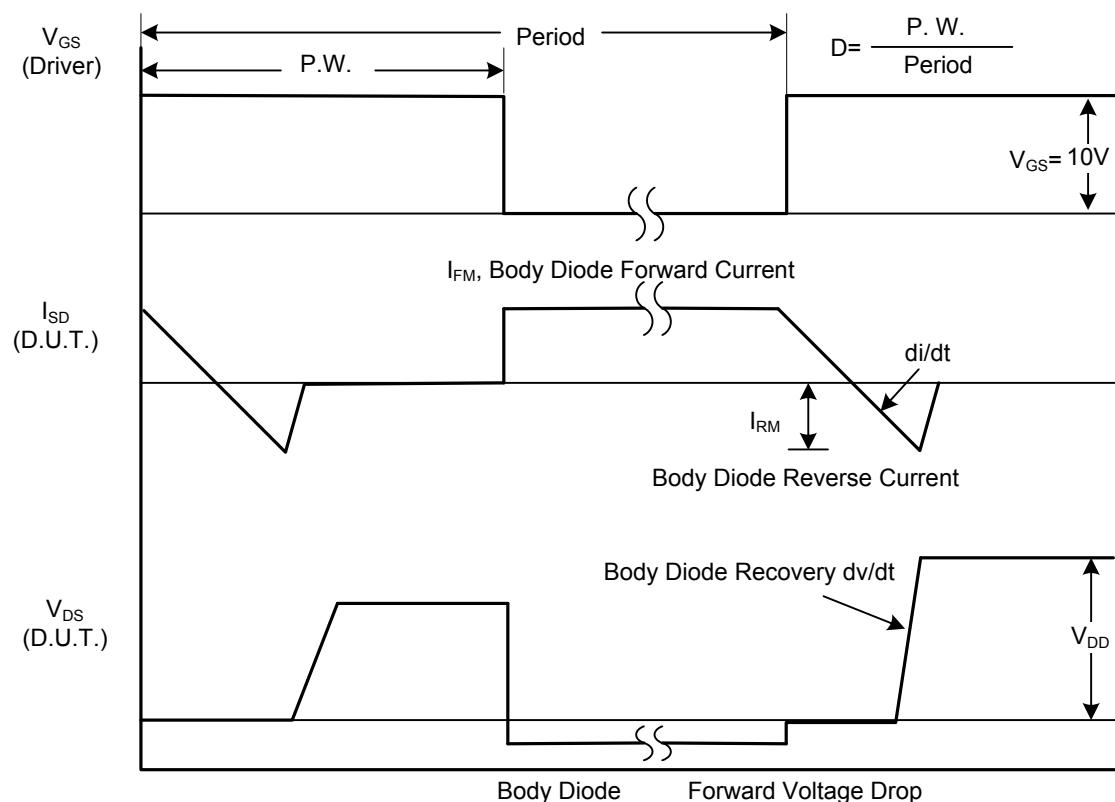
2. Essentially independent of operating temperature.



■ TEST CIRCUITS AND WAVEFORMS

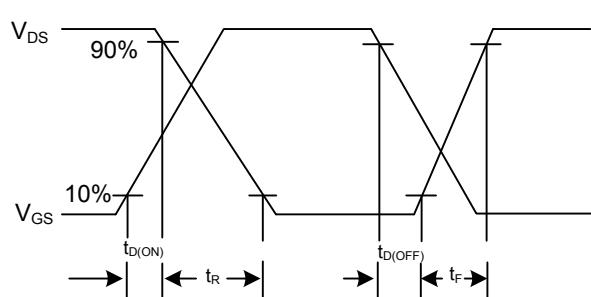
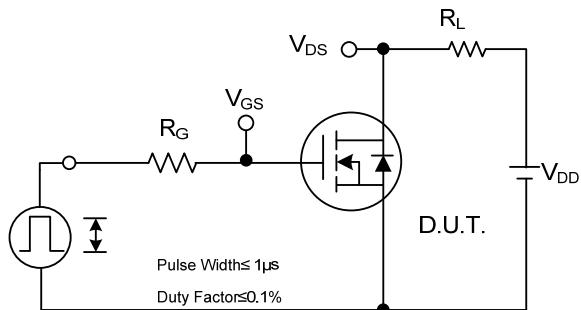


Peak Diode Recovery dv/dt Test Circuit



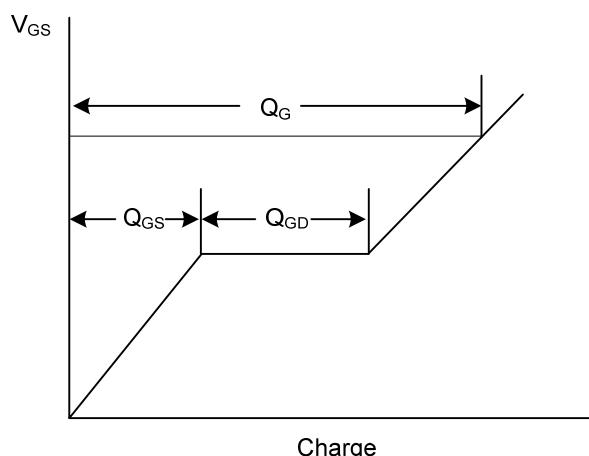
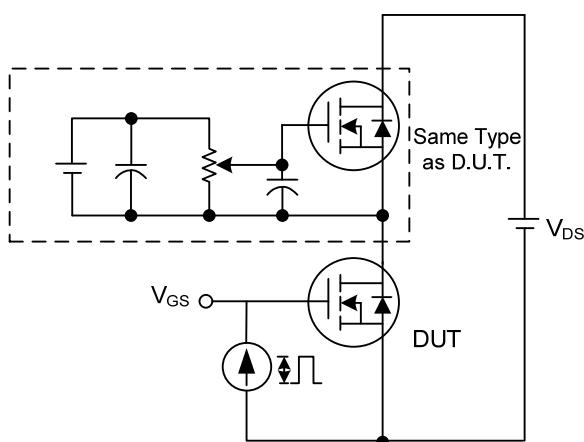
Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS



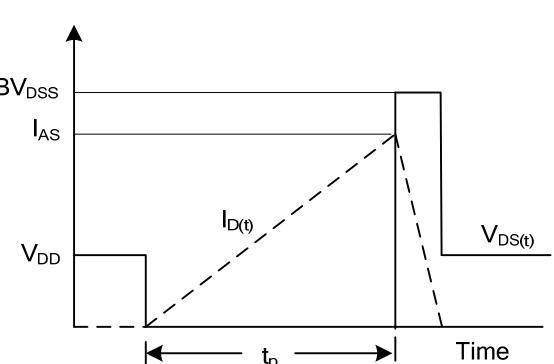
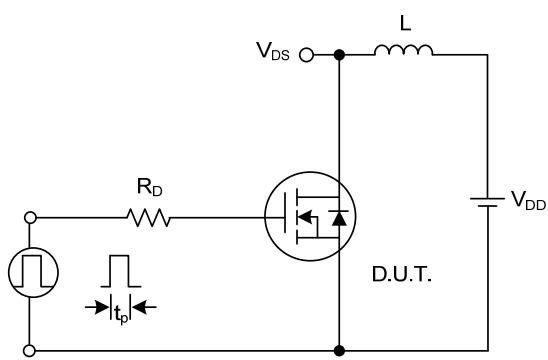
Switching Test Circuit

Switching Waveforms



Gate Charge Test Circuit

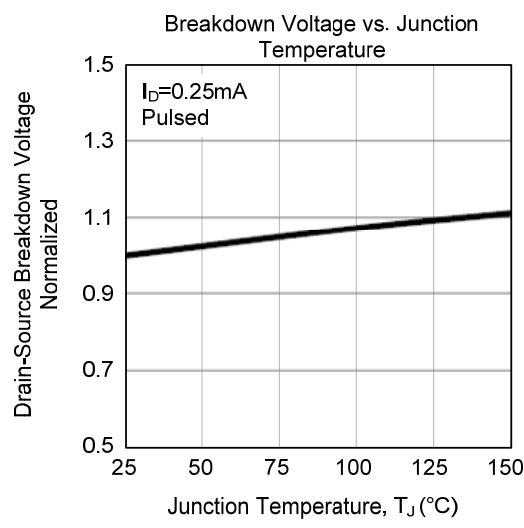
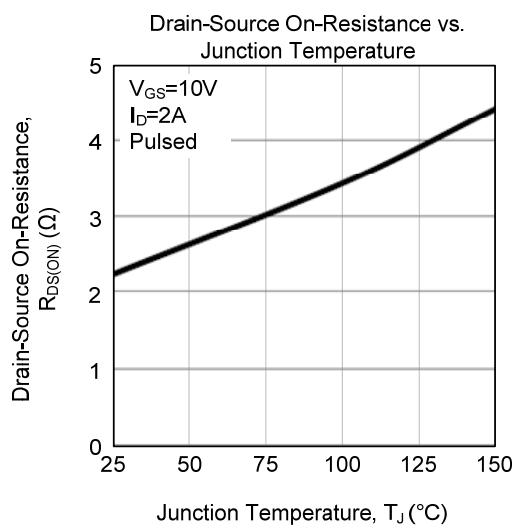
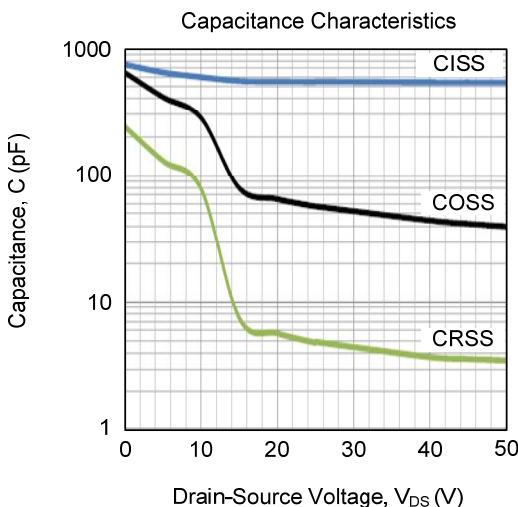
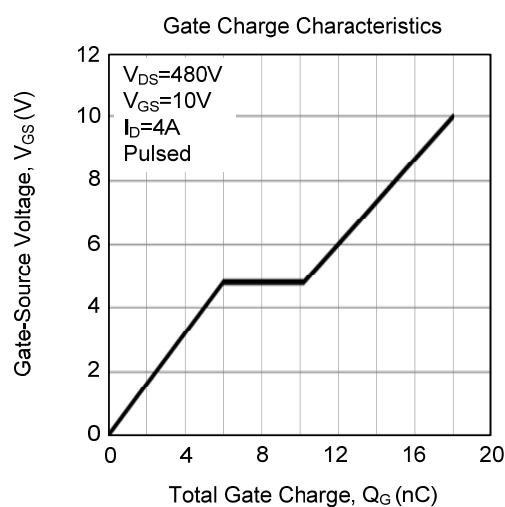
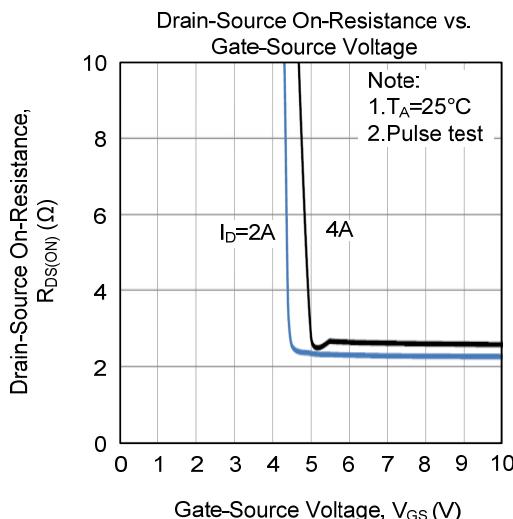
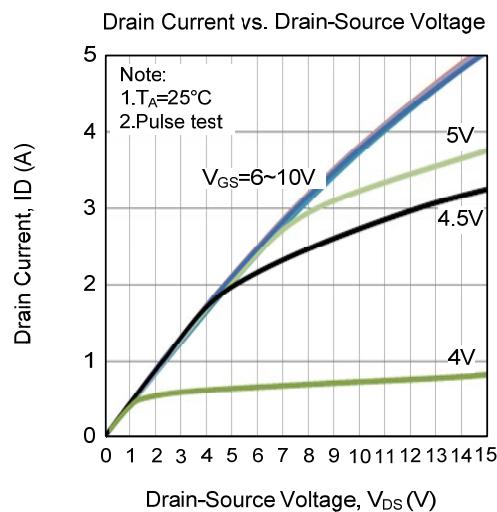
Gate Charge Waveform



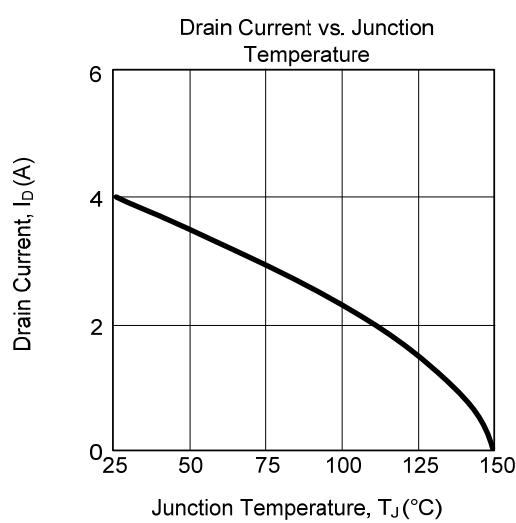
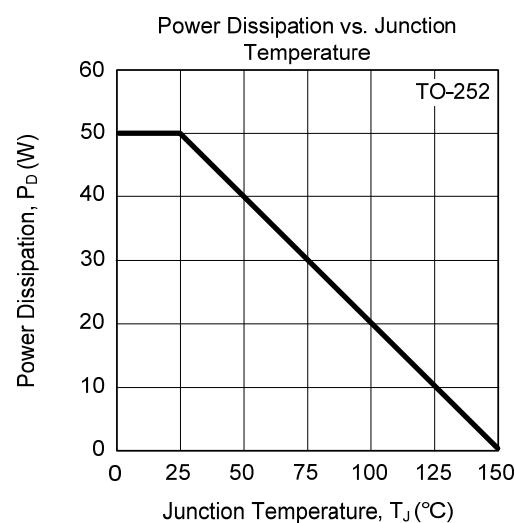
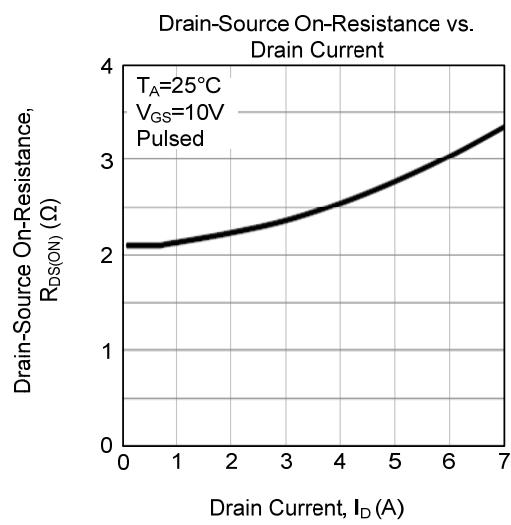
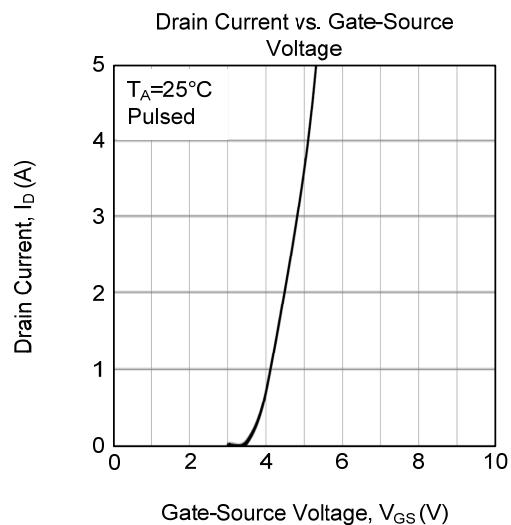
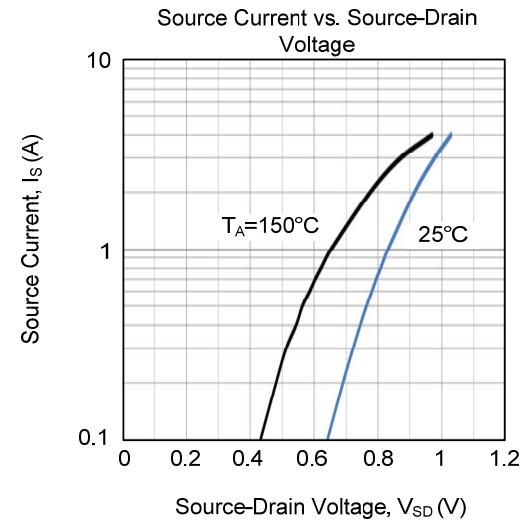
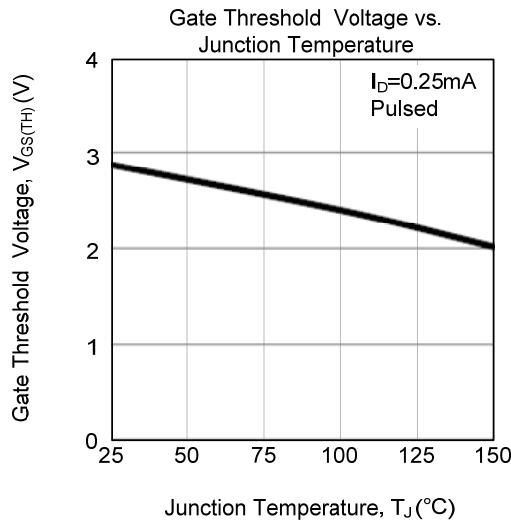
Unclamped Inductive Switching Test Circuit

Unclamped Inductive Switching Waveforms

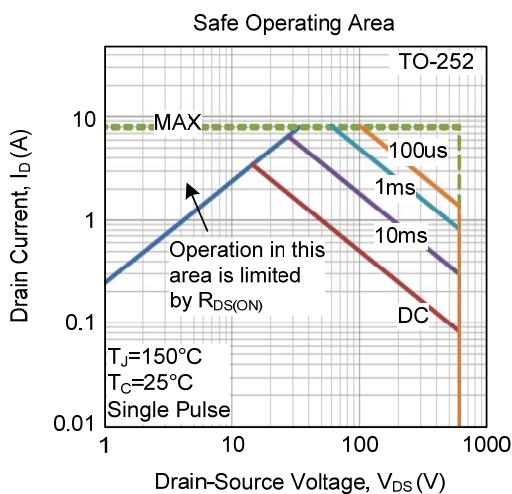
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



- TYPICAL CHARACTERISTICS (Cont.)



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